TANDY®

Cat. No. 26-252

TANDY 102

Technical Reference Manual

TANDY 102

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IMPORTANT NOTICE

This Technical Reference Manual is written for owners of the Tandy 102 Portable Computer who have a thorough understanding of electronics and computer circuitry. It is not written to the beginner's level of comprehension.

This manual contains detailed schematics and theories of operation for each major section of the Tandy 102. This information can aid you in designing interfaces for your computer, repairing it after the warranty expires, or simply obtaining practical knowledge of your Tandy 102 operation.

Radio Shack will not be liable for any damage caused, or alleged to be caused, by the customer or any other person using this technical manual to repair, modify, or alter the Tandy 102 Portable Computer in any manner.

Many parts of the computer electronics are very sensitive and can be easily damaged by improper servicing. We strongly suggest that for proper servicing, the computer be returned to Radio Shack.

Because of the sensitivity of computer equipment and the potential problems which can result from improper servicing, the following limitations apply to services offered by Radio Shack:

1. If any Radio Shack computer product has been modified so that it is not within manufacturer's specifications, including, but not limited to, the installation of any non-Radio Shack parts, components, or replacement boards, then Radio Shack reserves the right to refuse to service the equipment, void any remaining warranty, remove and replace any non-Radio Shack part found in the equipment, and perform whatever modifications are necessary to return the equipment to original factory specifications.

2. The cost for the labor and parts required to return the Radio Shack computer equipment to its original specifications will be charged to the customer in addition to the normal repair charges.

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Section 1. System Overview

The Tandy 102 is a portable computer equipped with built-in software to perform a variety of useful tasks such as text preparation, schedule and address organizing, and telecommunications.

Additionally, the Tandy 102 has the following standard features:

- Enhanced version of Microsoft BASIC
- Full-size typewriter-style keyboard
- LCD with eight lines by 40 columns
- Built-in modem
- Built-in cassette interface
- Built-in bar code reader interface
- Parallel printer interface

Other features available are: real time clock and calendar, upper- and lowercase characters, and RAM internally expandable to 32K bytes.

Specifications

Main Components

Keyboard

71 keys (9 x 8 matrix)

Alphabet keys	27
Number keys	10
Picture-control keys	7
Function keys	8
Special symbol keys	8
Mode keys	5
Other special-use keys	6

LCD

Display panel	240 × 64 full-dot matrix 1/32 duty 1/6.66 bias
Dot pitch	0.8 × 0.8 mm
Dot size	0.73 × 0.73 mm
Effective display area	191.2 × 50.4 mm

Operation batteries

Batteries	Four AA alkaline-manganese batteries
Operation time	5 days (at 4 hours/day) 20 days (at 1 hour/day) **Note: I/O is disconnected.**

Memory protection battery (on Main PCB)

Battery	Rechargeable
Protection time	About 20 days (16 kb) About 10 days (32 kb)
Recharge method	Trickle charge by AC adapter, or operation batteries

LSIs

CPU	80C85 Code and pin compatible with 8085
ROM	Max. 64kb (2 banks of 32 kb) Standard 32 kb Option 32 kb
RAM	Max. 32 kb Standard 24 kb RAM Incremental 8 kb RAM on PCB

Clock/Calendar	μPD1990AC No leap year/no February 29

I/O Interface

RS-232C (conforms to EIA Standard)

Signal	TXR (Transmit Data) RXR (Receive Data) RTS (Request to Send) CTS (Clear to Send) DSR (Data Set Ready) DTR (Data Terminal Ready)
Communications protocol	
Word length	6, 7, or 8 bits
Parity	NON, EVEN, or ODD
Stop Bit length	1 or 2 bits
Baud rate	75, 110, 300, 600, 1200, 2400, 4800, 9600, 19200 bits per second (bps)

Max. transmission distance	5m
Driver max. voltage output	± 5V
Driver min. voltage output	± 3.5V
Receiver max. voltage input	± 18V
Receiver min. voltage input	± 3V

Modem/coupler (conforms to BELL103 standards)

Baud rate	300 bps
Programmable items:	
Data length	6, 7, or 8 bits
Parity	NON, EVEN, or ODD
Stop bit	1 or 2 bits
Full duplex	Answer/call switchable mode
Other functions	Hang-up and auto-dialer

Audio cassette interface

Data rate	1500 bps (MARK: 2400 Hz, SPACE: 1200 Hz)

Printer interface (conforms to Centronics interface standards)

Handshake signal	$\overline{\text{STROBE}}$, BUSY, $\overline{\text{BUSY}}$

Controls and Functions

Power switch. Move this switch toward the front to turn the power ON. To conserve the batteries, the Tandy 102 automatically turns the power off if the unit is not used within 10 minutes. When an automatic power-off occurs, the switch remains in the ON position even though the power is off. To turn the power on, move the switch to the OFF position. then back to ON.

ANS/ORIG selector. This switch lets you select the modem answer mode or call mode. If you are originating a phone call to another computer, set the switch to ORIG. If another computer is calling your Tandy 102, set the switch to ANS.

DIR/ACP selector. This switch allows you to select either direct connection or acoustic coupler modem connection. If you are communicating with another computer by telephone via the build-in Direct Connect Modem, set the switch to the DIR position. If you are using the optional/extra Acoustic Coupler 2 (***Radio Shack Cat. No. 26-3818***), set the selector to the ACP position.

Memory power switch. This switch prevents over-discharge of the ni-cad battery for RAM back up. The Tandy 102 will not operate regardless of the setting of the power switch unless this switch is on. Set the switch to OFF if the Tandy 102 is not to be used for a long time. Note that the RAM will not be backed up when this switch is set to OFF.

RESET button. If the Tandy 102 "locks up" (i.e., the display "freezes" and all keys appear inoperative), press this button to return to the Main Menu (start-up) screen. It's highly unlikely that the Tandy 102 will lock up when you are using the built-in application programs. However, this situation may occur with customized programs.

Display adjustment dial. This control adjusts the contrast of the display relative to the viewing angle.

Special Function — Automatic Power OFF

When there is no program operation (awaiting command) for ten minutes, the power is automatically cut off.

To start again, the power switch must be turned OFF and then ON, thus releasing the automatic power OFF condition. (The display will be the same as before the power was turned off.)

Connectors

RS-232C	25 pins (DB-25S)
Printer	26 pins (FRC5-C26-L33-ON)
Modem	8 pins (TCS-4490)
Cassette	8 pins (TCS-4480)
Bar code reader	9 pins (A-7224)
System bus	40 pins (Hu-400S2B-L13TB4)
AC adapter	5.5 (Center Minus)

Section 2. Theory of Operation

The Tandy 1Ø2 has three principal LSIs:

- 8ØC85 Central Processing Unit (CPU) that controls all functions
- 81C55 Parallel Input/Output (PIO) interface controller that controls the parallel printer, keyboard, buzzer, clock and display
- IM64Ø2 Universal Asynchronous Receiver Transmitter (UART) that controls the serial interface (RS-232C or modem)

The block diagram shows the various internal components and connections of the Tandy 1Ø2

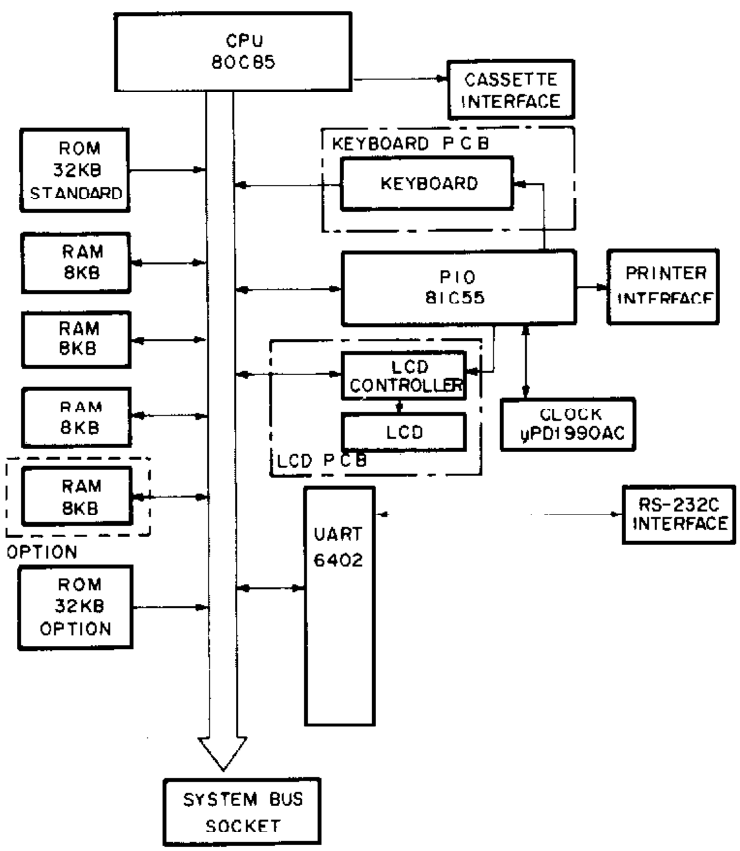


Figure 2-1. System Block Diagram

The input/output for a cassette recorder and the input of the BCR are controlled by the CPU directly through its SOD, SID, and RST 5.5 terminals.

ROM and RAM are connected to the system bus. ROM is available only for alternative selection of standard or optional.

Technical Description

The technical description of the Tandy 102 is divided into 17 sections:

- Processor
- Memory
- Address Decoding and Bank Selection
- Memory Map
- I/O Map and I/O Port Description
- Keyboard Control Circuit
- Cassette Interface Circuit
- Printer Interface Circuit
- Bar Code Reader Interface
- Buzzer Control Circuit
- System Bus
- LCD Interface Circuit
- Clock Control Circuit
- Serial Interface Circuit
- Liquid Crystal Display
- Power Supply and Automatic Power OFF Circuit
- Reset Circuit

This breakdown, which corresponds with the partitioning of the schematic diagrams, will allow easy explanation and referencing.

Processor

The Tandy 102 uses an MSM80C85ARS (80C85) CPU chip, a complete 8-bit parallel central processing unit. With an instruction set that is 100 percent software-compatible with the 8080A microprocessor, 80C85 represents an improvement over 8080A's performance with a higher system speed.

80C85 uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus.

The data and address buses are separated by M1 (TC40H373F: Octal "D" type latch). The performance of the bus line is increased by M2 (TC40H245F: Octal bidirectional bus buffer) and M20, M21 (TC40H367F: Octal buffer/driver).

Memory

The Tandy 102's memory consists of a 32K ROM and up to 32K of RAM (standard RAM is 24K). The memory can be expanded to 32K with the addition of one 8K RAM. Also, an additional (optional) 32K ROM can be installed.

Random Access Memory (RAM)

The standard RAM for the Tandy 102 is M9, M8, and M7. Memory capacity can be increased up to 32K, however, by installing M6.

Read Only Memory (ROM)

The Tandy 102 uses a synchronous 32K ROM (256K bits). Operated by a single 5-volt power supply, the access time is 150nsec (max). The BASIC program is stored in the standard ROM. The BIOS program is stored in the standard ROM for operation of the display, printer, etc.

An optional ROM can be installed in the special IC socket by removing the ROM cover on the bottom case of the Tandy 102. A variety of application programs can be entered in the optional ROM.

Address Decoding and Bank Selection

RAM Chip Selection. Although four 8K RAM packs can be installed in the Tandy 102, 16 chip-select signals are necessary since 16 × 2K RAMs are actually used.

Moreover, because the RAM area is addressed from 8000H to FFFFH (see Figure 2-2), the control signal is formed by IO/$\overline{M}$, A15 and A14 as shown in Figure 2-2. The 16 chip-select signals are formed by A13, A12, and A11.

M5 (TC40H139: dual 2 to 4-line decoder/demultiplexer) generates the control signal. M3 and M4 (TC40H138: 3 to 8-line decoder/demultiplexer) generate the 16 chip-select signals.

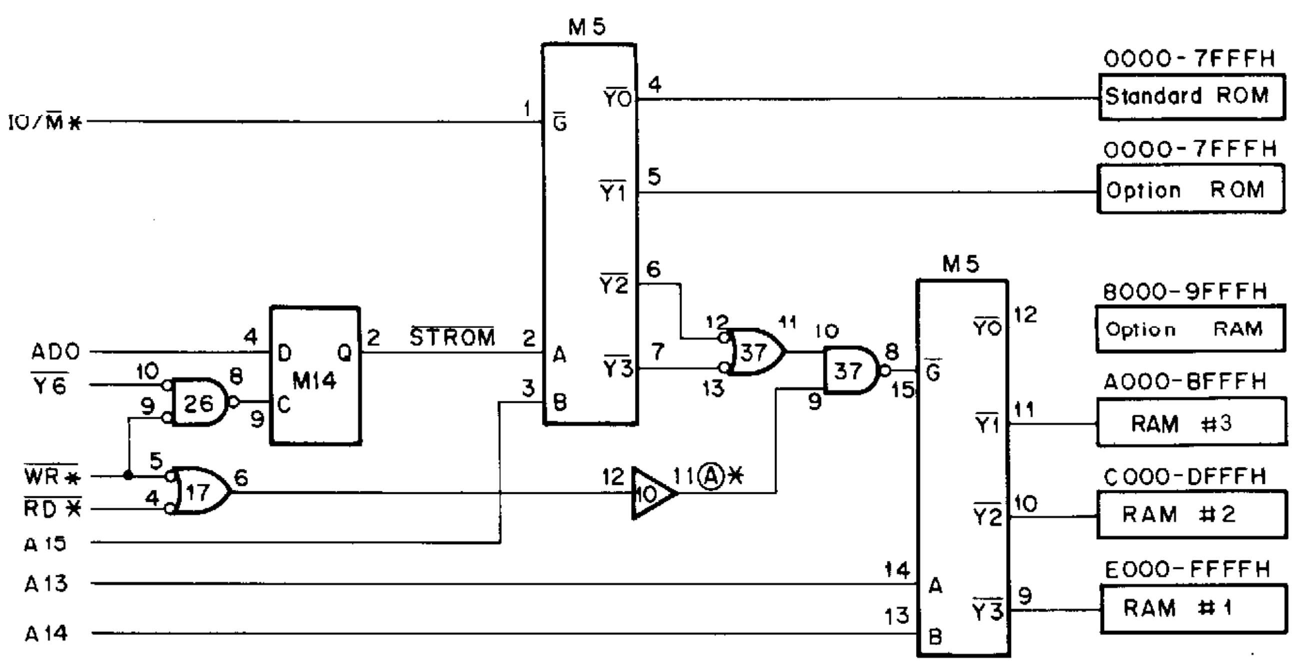


Figure 2-2. Address Decoding and Bank Selection Circuit

ROM Chip Selection. ROMs (both standard and optional) used in the Tandy 102 are the 32K 1-chip type. As shown on the Memory Map in Figure 2-3, the address space is positioned from 0000H to 7FFFH.

Chip-select signals are generated by A15 and $\overline{\text{STROM}}$.

AD0 is latched at M14 (TC40H175 quad "D" type F/F) by signals $\overline{WR}$ and $\overline{Y6}$, then $\overline{STROM}$ is generated. (Refer to the I/O port description.)

The chip-select signal of each ROM is generated by an IO/$\overline{M}$ signal at M5 (TC40H139). The standard ROM is selected by the L $\overline{STROM}$ signal and the optional ROM by the H $\overline{STROM}$ signal.

Memory Map

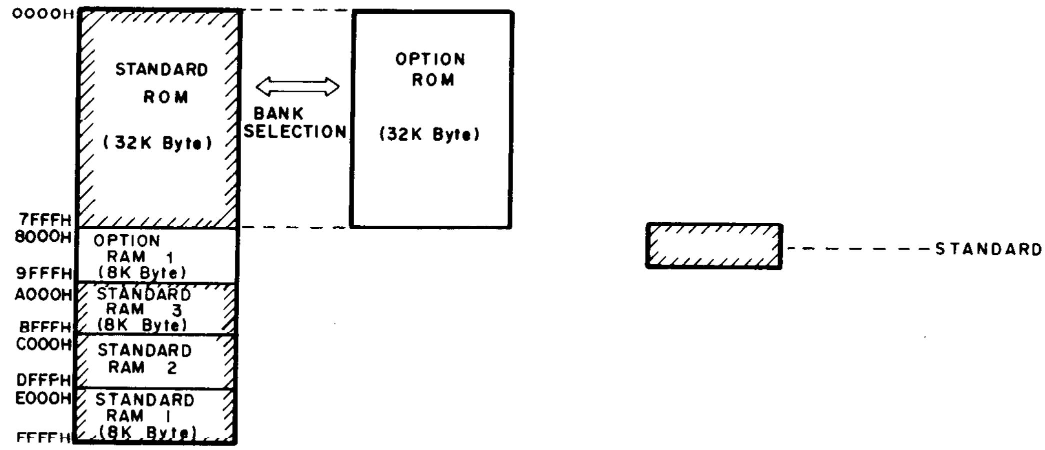


Figure 2-3. Memory Map

I/O Map and I/O Port Description

As shown in Figure 2-4, the I/O address decoder circuit, consisting of M-16 (40H138), decodes address signals A12 to A15 and generates the I/O control signals $\overline{Y0}$ to $\overline{Y6}$ and $\overline{Y7}$.

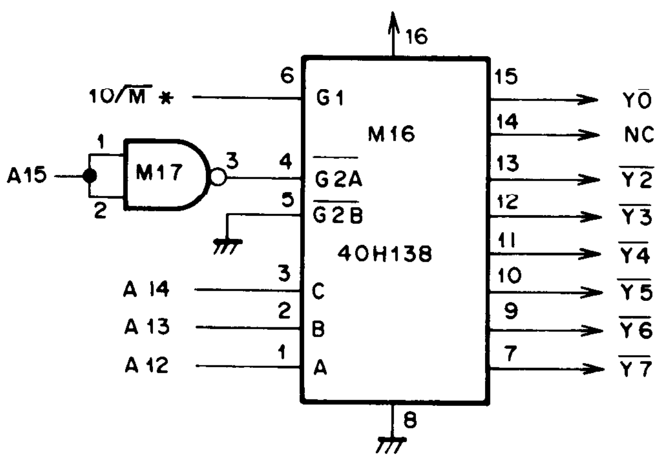


Figure 2-4. I/O Address Decoding Circuit

Because the liquid crystal display (LCD) driver-select signal $\overline{Y7}$ is active low (L), the output of M16 (40H138) is inverted by M17 (40H000). Table 2-1 shows how select signals ($\overline{Y0}$ to $\overline{Y6}$ and $\overline{Y7}$) for the I/O device and address are used.

Address	Signal	Active Level	Application
00H-7FH	—	—	Free area for optional unit and other select signals of circuits made by user
80H-8FH	$\overline{Y0}$	L	Device-select signal for optional I/O controller unit.
A0H-AFH	$\overline{Y2}$	L	Bit 0: ON/OFF of relay for signal selection of telephone unit. Bit 1: Generates ENABLE signal of LSI (MC14412) for MODEM.
B0H-BFH	$\overline{Y3}$	L	PIO (81C55) chip-select signal.
C0H-CFH	$\overline{Y4}$	L	ENABLE signal for data input/output port of UART (IM6402).
D0H-DFH	$\overline{Y5}$	L	ENABLE signal to set various modes and read port of UART.
E0H-EFH	$\overline{Y6}$	L	ENABLE signal for $\overline{\text{STROM}}$ and REMOTE, and input data from keyboard. Also, strobe signal for printer and clock.
F0H-FFH	$\overline{Y7}$	L	ENABLE signal for LCD driver LSI

Table 2-1. I/O Map

Table 2-2 shows the I/O address of each port of PIO (81C55)

Address	Port or Register
B0H or B8H	Command/status (Internal)
B1H or B9H	Port A
B2H or BAH	Port B
B3H or BBH	Port C
B4H or BCH	Timer register lower byte
B5H or BDH	Timer register upper byte
B6H, B7H, B8H, and B9H	Not used

Table 2-2. I/O Address of Each Port

Keyboard Control Circuit

Key strobe signals PB0 and PA0 - PA7 are generated by the 81C55, and the return signals from the keyboard pass through the octal bus buffer IC (40H367) to the CPU. Data input port I/O address at this time is E0H - EFH. The keyboard control circuitry is shown in Figure 2-5. This figure shows the circuit condition when (T) is pressed.

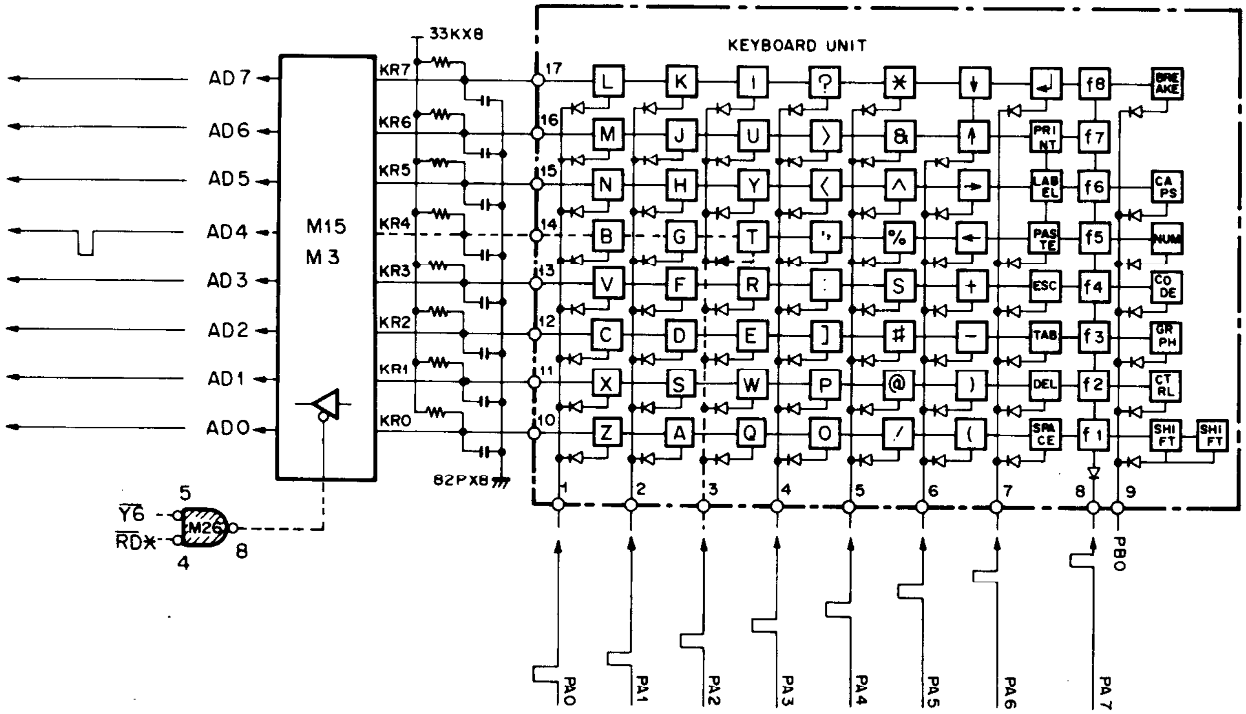


Figure 2-5. Keyboard Control Circuit (on Pressing (T))

Cassette Interface Circuit

The cassette interface circuitry is divided into three sections:

- Modulation
- Demodulation
- Remote

In modulation, serial data is modulated and converted into a recording signal. The playback signal is demodulated and converted into a digital signal in demodulation. And, the remote is the part of the circuit that enables or disables the recorder's motor.

Modulation

Modulation is accomplished in several steps. First, serial data from the SOD terminal of the CPU is inverted (by M34). Next, the DC component is removed (by C63). Then, data passes through an integrator (consisting of R51 and C64) and, after voltage division, out to a recorder microphone input. Figure 2-6 shows the modulation circuit of the cassette interface.

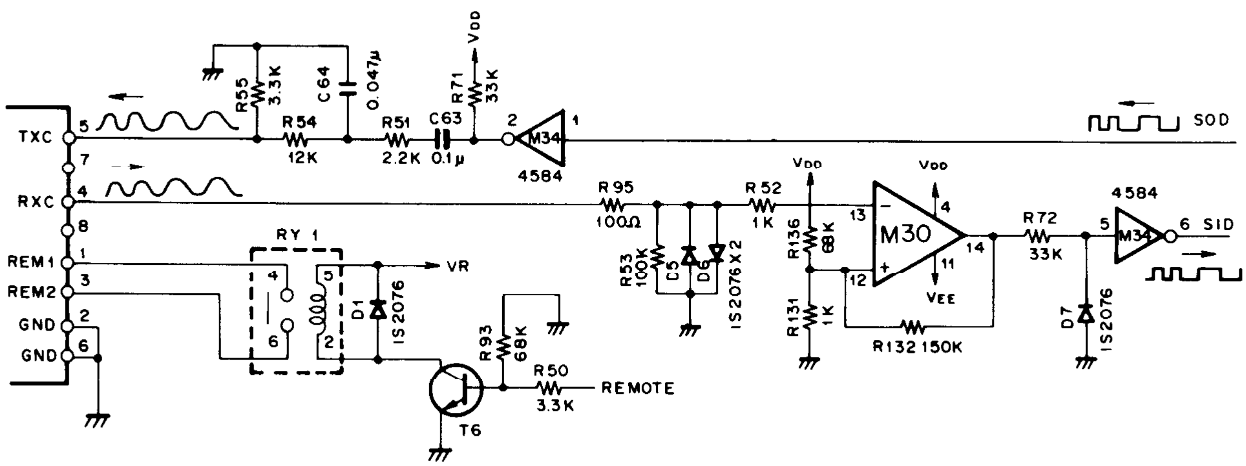


Figure 2-6. Cassette Interface Circuit

Demodulation

The signal input from the earphone jack of the recorder passes through the D5 and D6 clamp circuit, and is then emitted from a comparator circuit composed of an operation amplifier IC (TL64, M30). The input signal is converted into a digital signal and applied to the SID terminal of the CPU. Figure 2-6 shows the demodulation circuit of the cassette interface.

In this circuit, D7 clamps the negative voltage output of the comparator.

Remote

The $\overline{\text{REMOTE}}$ signal output is changed to L level as a result of the write-in of data 1 to bit 3 of the output port (40H175: M14) specified by I/O addresses E0H - EFH. As a result, T6 switches ON, the relay (RY1) is energized, and the recorder controls begin to operate. Figure 2-6 shows the remote circuit of the cassette interface.

Printer Interface Circuit

The printer interface circuit conforms to Centronics standards. As shown in Figure 2-7, the BUSY signal from the printer is read from PC2 of 81C55. If the condition is NOT BUSY (PC2: L level), the 8-bit data is sent to PA0 - PA7 of 81C55. Then, as a result of data 1 write-in to bit 1 of the output port (40H175: M14), indicated by I/O address E0H - EFH, T8 is switched ON and the L level $\overline{\text{STROBE}}$ signal is sent to the printer.

When the printer receives the $\overline{\text{STROBE}}$ signal, the BUSY signal is changed to H level, indicating that the printer is busy. The CPU then waits until the BUSY signal reaches the L level. When the BUSY signal reaches L level, the CPU ends the output of PA0 - PA7 data of 81C55, and the output of 1 byte of print data is completed.

If the printer is ON LINE, the $\overline{\text{BUSY}}$ signal is H level. But, if the printer is OFF LINE, the signal becomes L and transmission of print data to the printer is not possible.

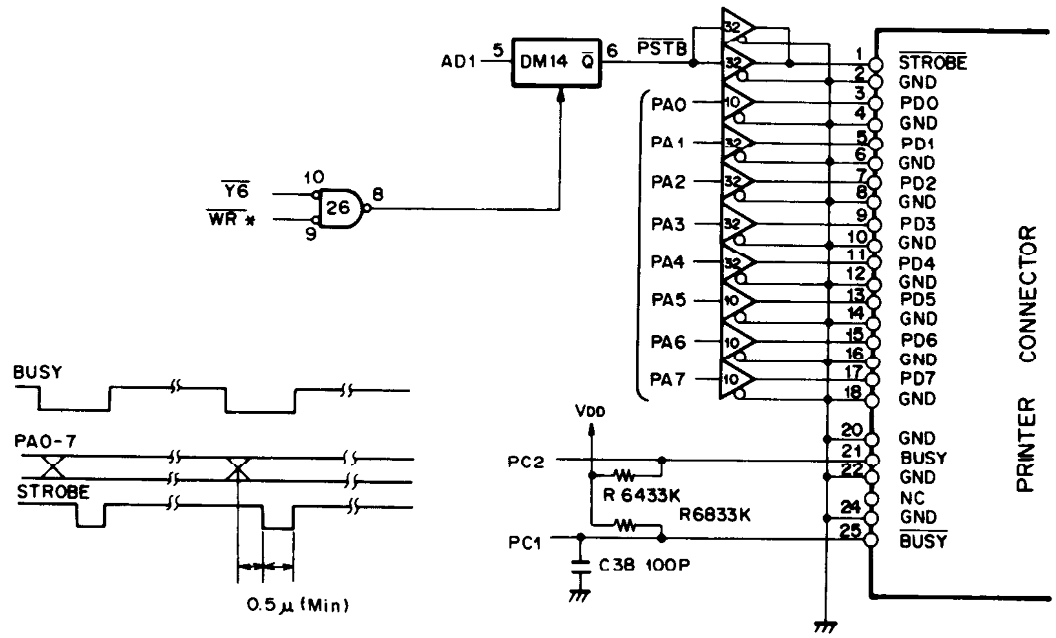


Figure 2-7. Printer Interface Circuit

Bar Code Reader Interface

The input signal from the bar code reader is subjected to waveform shaping, inverted by the Schmitt type inverter (M34), then delivered to the 81C55 PC3 and 80C85 RST 5.5 terminals.

When the bar code reader reads the first white part of the bar code, the L signal is generated, then inverted by M34. As soon as RST 5.5 interaction occurs, data input starts.

As the bar code reader is moved across the bar codes, H and L signals are generated to correspond to the white and black areas, respectively. Finally, the inversion signals are input to PC3 of 81C55 as serial data. Figure 2-8 shows the bar code reader interface circuit.

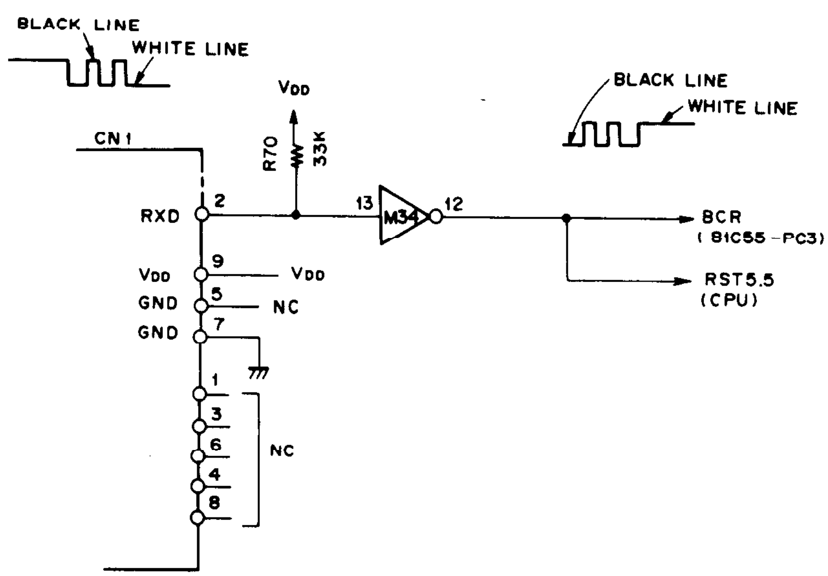


Figure 2-8. Bar Code Reader Interface Circuit

Buzzer Control Circuit

There are two ways to activate the buzzer. One is by emitting a signal from PB5 of 81C55 at a particular frequency; the other, by using the timer output of 81C55.

Signal from PB5 of 81C55

When PB2 of 81C55 is H level, the buzzer is made to sound by repeatedly switching the buzzer drive transistor ON and OFF. This is accomplished by the H, L, H, L . . . signals of output from PB5 synchronizing with the frequency for sounding the buzzer.

81C55 Timer Output

In this method, the buzzer is made to sound by setting the 81C55 timer in the square wave output mode and the value corresponding to the frequency which will sound the buzzer. With PB5 at H level, the buzzer will sound whenever PB2 is switched to L. This causes the square-wave pulse emitted from the timer out (TO) terminal of 81C55 to be applied to the base of the transistor for buzzer drive. PB2 uses this as the buzzer ON/OFF control signal.

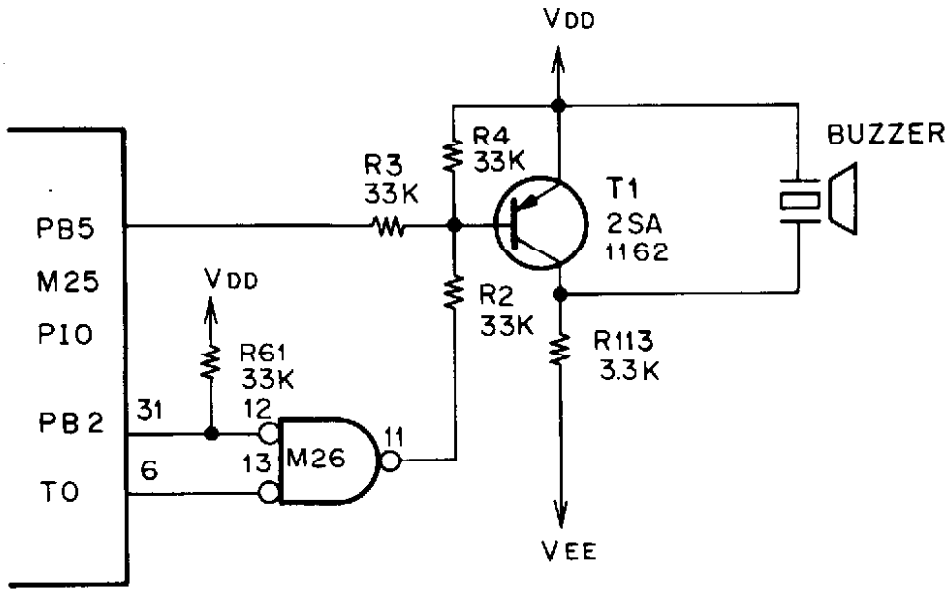


Figure 2-9. Buzzer Control Circuit

System Bus

To expand the use of external devices, the system bus is tied to a 40-pin connector. As shown in Table 2-3, the 80C85 address bus, data bus, and control bus, can all be connected to the external system from the system bus, making system expansion easy. In addition, the optional I/O control unit and RAM file can be connected to this system bus.

Pin No.	Signal	Description
1	**VDD**	+5V power supply
2	**VDD**	+5V power supply
3	**GND**	Ground
4	**GND**	Ground
5	**AD0**	Address and data signal bit 0
6	**AD1**	Address and data signal bit 1
7	**AD2**	Address and data signal bit 2
8	**AD3**	Address and data signal bit 3
9	**AD4**	Address and data signal bit 4
10	**AD5**	Address and data signal bit 5
11	**AD6**	Address and data signal bit 6
12	**AD7**	Address and data signal bit 7
13	**A8**	Address signal bit 8
14	**A9**	Address signal bit 9
15	**A10**	Address signal bit 10
16	**A11**	Address signal bit 11
17	**A12**	Address signal bit 12
18	**A13**	Address signal bit 13
19	**A14**	Address signal bit 14
20	**A15**	Address signal bit 15
21	**GND**	Ground
22	**GND**	Ground
23	**RD***	Read enable signal
24	**WR***	Write enable signal
25	**IO/M***	I/O or memory select signal
26	**S0**	Status 0 signal
27	**ALE***	Address latch enable signal
28	**S1**	Status 1 signal
29	**CLK**	Clock signal
30	**Y0**	I/O controller select signal
31	**A***	I/O or memory access enable signal
32	**RESET***	Reset signal
33	**INTR**	Interrupt request signal
34	**INTA**	Interrupt acknowledge signal
35	**GND**	Ground
36	**GND**	Ground
37	**RAM RST**	RAM enable signal
38	**NC**	No connection
39	**NC**	No connection
40	**NC**	No connection

Table 2-3. System Bus Pin Assignments

Table 2-4 shows the DC characteristics of each system bus signal.

Item	Characteristics
High-level output voltage (VOH)	4.95V min (IOH < 1μA)
Low-level output voltage (VOL)	0.05V max (IOL < 1μA)
High-level output current (IOH)	-0.88mA min (VOH = 4.6V)
Low-level output current (IOL)	4.4mA min (VOL = 0.4V)
High-level input voltage (VIH)	4.0V min (IOH < 1μA)
Low-level input voltage (VIL)	1.0V max (IOL < 1μA)

Table 2-4. System Bus DC Characteristics

Note: Values shown in Table 2-4 are for normal temperature (Ta = 25°C) and power (VDD = 5.0V).

LCD Interface Circuit

The LCD interface circuit links the LCD driver to the CPU. See Figure 2-10.

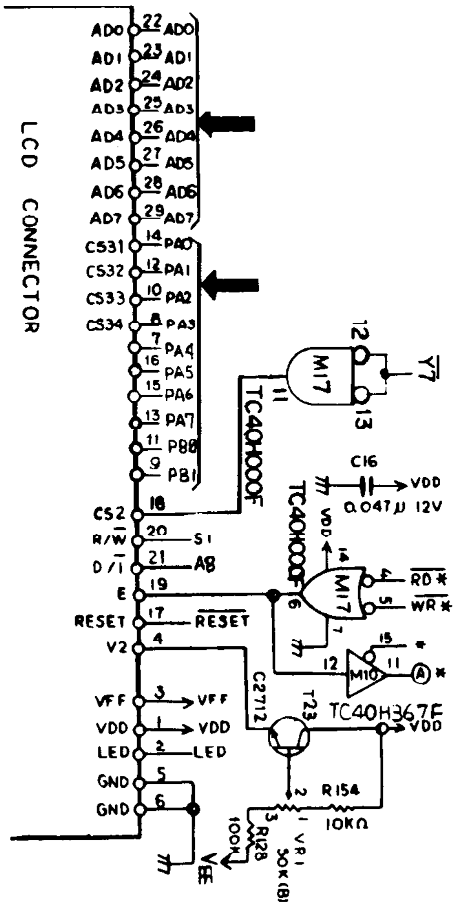


Figure 2-10. LCD Interface Circuit

The following signals are necessary for LCD driver interface:

AD0 - AD7	For write-in of control data or display data to the LCD driver. Signal line for read-out from the driver.
Y7	LCD driver enable signal
PA0 - PA7, PB0, PB1	Chip enable signal for each LCD driver
S1	Indicates whether data is being written into the LCD driver (S1 = L) or read out (S1 = H)
A8	Register-select signal in the LCD driver. AD0 - AD7 are display data when A8 = H; and command, or status data, when A8 = L.
E	NAND output signal of $\overline{RD}$ signal and $\overline{WR}$ signal. Indicates the timing of the LCD driver data read/write.
V2	Voltage to keep the LCD driver voltage standard. LCD display can be changed by changing the V2 voltage by VR2.

Figure 2-11 shows the operating timing of each signal. Refer to the LCD PCB technical description for detailed characteristics and operation of the LCD and LCD driver.

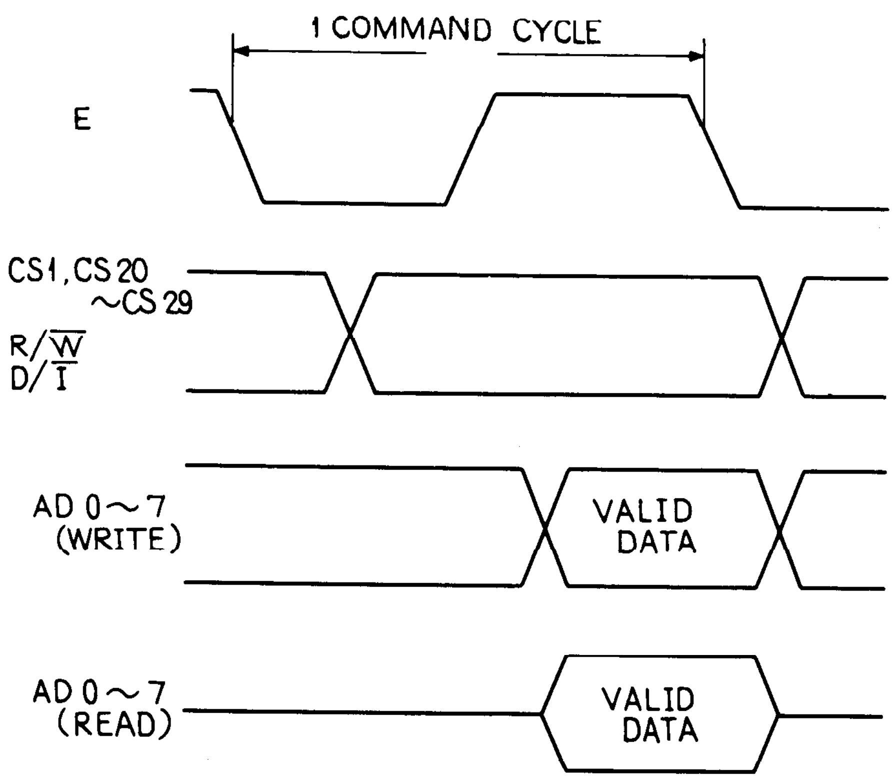


Figure 2-11. LCD Interface Timing Chart

Clock Control Circuit

A clock LSI (μPD1990AC) is used in the clock control circuit so that the time can be set and read through BASIC commands.

When the Tandy 102 is in the operable condition (RESET is H level), commands and data can be input and output to μPD1990AC (M18) from the CPU at will.

In addition, because battery voltage VB is applied to the μPD1990AC, the clock functions even when Tandy 102's power switch is OFF.

The clock's LSI C0 - C2, DATA IN and CLK terminals are connected to the 81C55 PC0 terminal. The STB signal is provided from bit 2 of output port made by M14 (40H175).

The TP output signal is connected to the RST 7.5 interruption input terminal of the CPU. Square waves are output from the TP (4 ms cycle), and one key scan occurs every 4 ms because of the RST 7.5 interruption to the CPU.

Time Set Sequence

The CPU sets μPD1990AC to the register shift mode with the 100 pattern of C0 - C2 and the strobe signal which is generated by AD2, $\overline{Y6}$ and $\overline{WR}$ signals applied to M14. Then, the CPU sends the time and date information to the DATA IN terminal of μPD1990AC with timing clock (PA3). Finally, the CPU sets the time set mode with the 010 pattern of C0 - C2 and the strobe signal. See Figure 2-12.

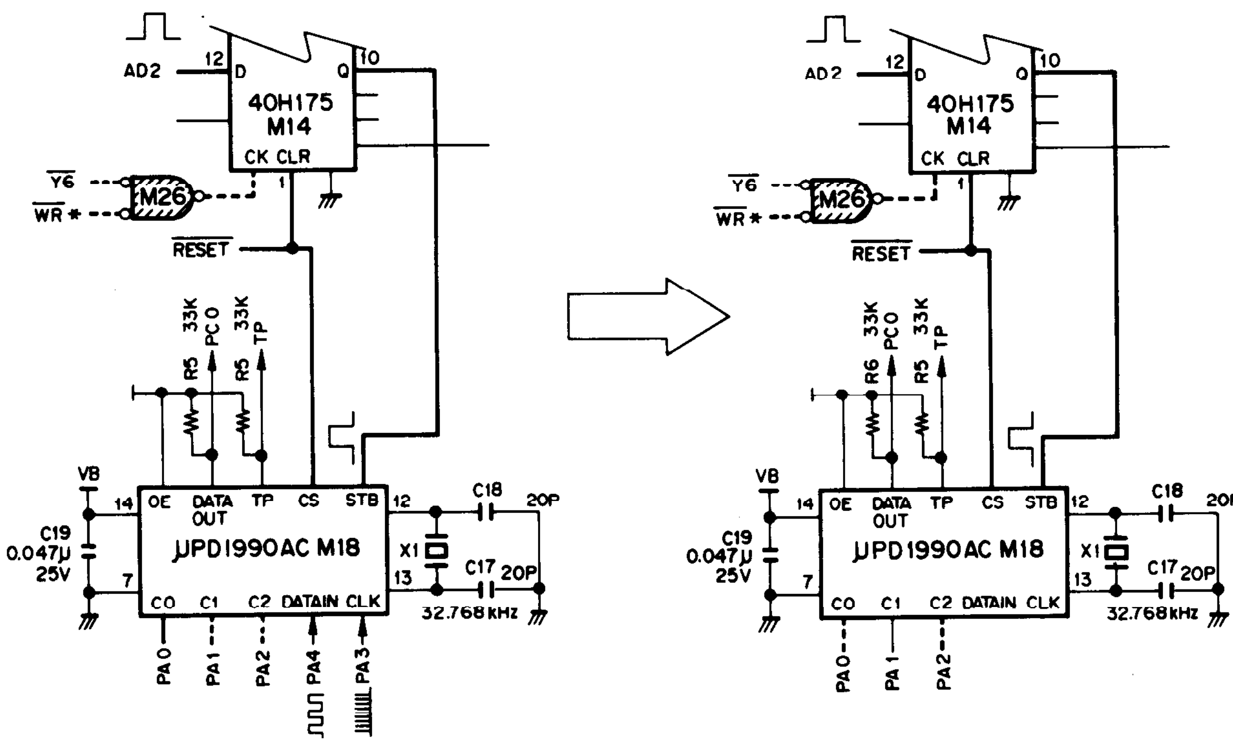


Figure 2-12. Time Set Sequence of μPD1990AC

Time Read Sequence

The CPU sets μPD1990AC to the time read mode with the 110 pattern of C0 - C2, and the strobe signal. The CPU sets to the register shift mode again with the 100 pattern of C0 - C2, and reads the time and date information from the DATA OUT terminal. At the same time, the CPU sends the PA3 signal passing through 81C55 for the timing clock. See Figure 2-13.

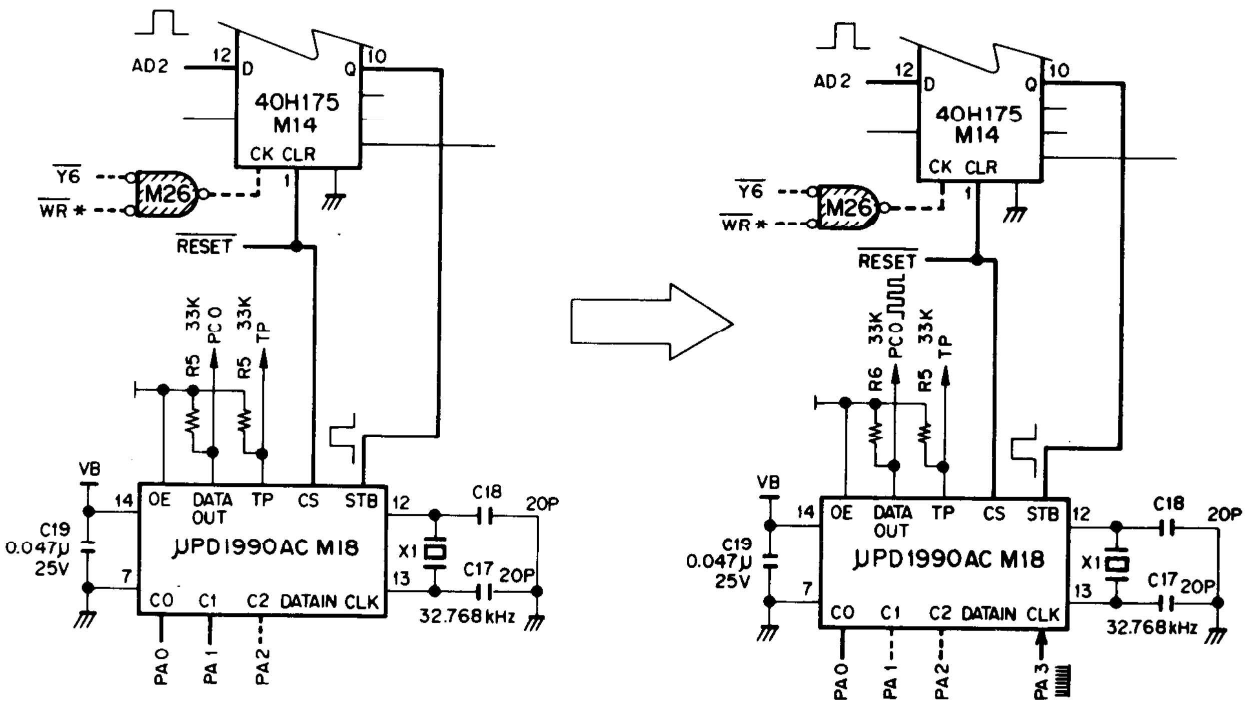


Figure 2-13. Time Read Sequence of μPD1990AC

Serial Interface Circuit

The serial interface circuit is divided into three parts — serial control, RS-232C interface, and modem. This circuit controls the changes and transmission/reception of data (parallel and serial data) between the CPU, the modem, and the RS-232C circuits.

Serial Control Circuit

Serial control is performed by the UART LSI (IM6402). The CPU begins data transmission/reception after the control word that determines the mode (transmission/reception) is written into the control register selected by the $\overline{Y5}$ signal.

For transmission, the condition of the IM6402 TBRE signal from bit 4 of the status input port (M4, M23), selected by the $\overline{Y5}$ signal, is read. If the signal is L, the chip waits until the signal becomes H.

When the TBRE signal becomes H, data transmission is possible. If the transmission data is written into the transmitter buffer register (TBR1 - TBR8), the data is output as serial data, containing the start, parity, and stop bits from the TRO terminal.

For reception, when data enters the RRI terminal, the DR terminal changes from L to H and the RST 6.5 interruption notifies the CPU that the IM6402 has received data.

The CPU reads the OE, FE, and PE signals from the status input port (M4, M23). If there is no error when the serial data is received, the received data from the receive buffer register selected by $\overline{\text{Y4}}$ can be read as 8-bit parallel data.

The IM6402 serial transmission/reception reference clock signal is taken from the TO terminal by setting the 81C55 timer.

In addition, the status input port bit 5 RP signal is held as an option for modem operation.

Table 2-5 shows the signal correspondence between the data bus, status bit, and control register of IM6402.

Data bus	Control register	Status bit
AD0	SBS (Stop Bit Select)	–
AD1	EPE (Even Parity Enable)	OE (Overrun Error)
AD2	PI (Parity Inhibit)	FE (Framing Error)
AD3	CLS1 (Character Length Selected 1)	PE (Parity Error)
AD4	CLS2 (Character Length Selected 2)	TBRE (Transmitter Buffer Register Empty)
AD5	–	–
AD6	–	–
AD7	–	–

Table 2-5. Status Bit and Control Register of IM6402

MODEM/RS-232C Exchange Circuit

Because the serial input/output port which forms IM6402 is one channel only, the circuit shown in Figure 2-14 is multiplexed to $\overline{\text{RS-232C}}$ and the MODEM.

The $\overline{\text{RS-232C}}$ signal (PB3 terminal of 81C55) determines whether the serial port is to be used as RS-232C or as a modem. When the $\overline{\text{RS-232C}}$ signal is L, the serial port is used as RS-232C. When it is H, the port is used as MODEM.

The reception signal, including the control signal, is demultiplexed at 40H157 (M33). The transmission signal is multiplexed at M24 and M26.

$\overline{\text{CTS}}$ and $\overline{\text{DSR}}$ signals (as the serial port) are input to PC4 and PC5 of 81C55. The CD signal is input from bit 0 of the status input port (M23). Output signals $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ are output from PB6 and PB7 of 81C55.

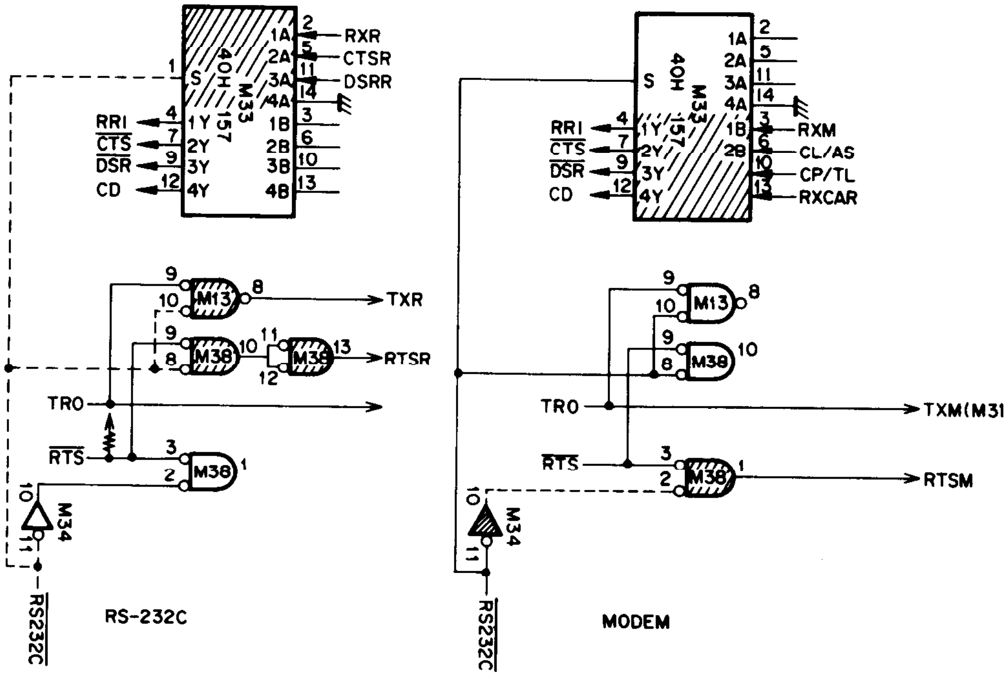


Figure 2-14. RS-232C/MODEM Selection Circuit

RS-232C Interface Circuit

In the RS-232C transmission circuit, after the DC component is removed from the IM6402 TRO, $\overline{RTS}$, and $\overline{DTR}$ signals by the coupling capacitor (0.039 µF 50V), the signals are leveled to + −5V signals by the Schmitt trigger type inverter IC (M35), and then are output as RS-232C transmission signals.

In the RS-232C reception circuit, DSRR, CTSR, and RXR signals from the external RS-232C line are subjected to waveform shaping and inverted by M35 and diode IS1535, and then converted to +5V or GND level signals. The signals are then demultiplexed by 40H157 (M33) and converted to $\overline{CTS}$, $\overline{DRS}$, and RRI signals which can be controlled by the CPU. See Figure 2-15.

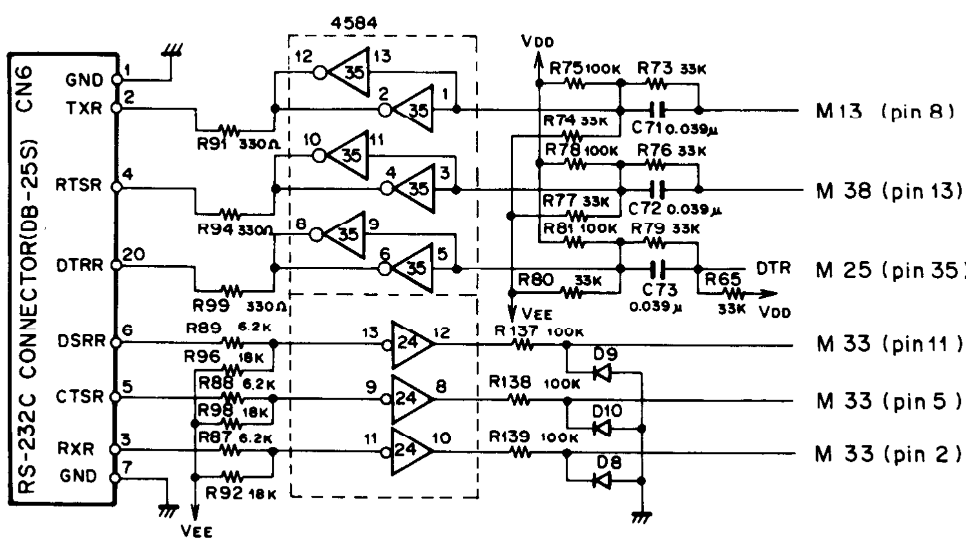


Figure 2-15. RS-232C Interface Circuit

Table 2-6 shows the application of each signal of the RS-232C circuit.

Symbol	Name	Application
TXR	Transmit Data	Data Output from RS-232C
RXR	Receive Data	Data Input to RS-232C
RTSR	Request to Send	
CTSR	Clear to Send	
DSRR	Data Set Ready	
DTRR	Data Terminal Ready	

Table 2-6. RS-232C Signals

Modulation/Demodulation IC and Peripheral Circuit

Modem circuitry consists of the modulation/demodulation IC, transmission filter, reception filter, and other circuits.

The Rx Rate and Type terminals of MC14412 (M31) are pulled up to VDD. Baud rate is set to 300 bps and the U. S. standard is selected. Since the ECHO and SELF TEST terminals are not needed, they are grounded. The Q output (En signal) of the port (M36) selected by bit 1 of the Y2 port is input to the ENABLE terminal until the unit is in the MODEM mode.

In addition, the signal designated by the ORIG/ANS switch is input to the MODE input, and switches between the Originate or the Answer mode. See Figure 2-16.

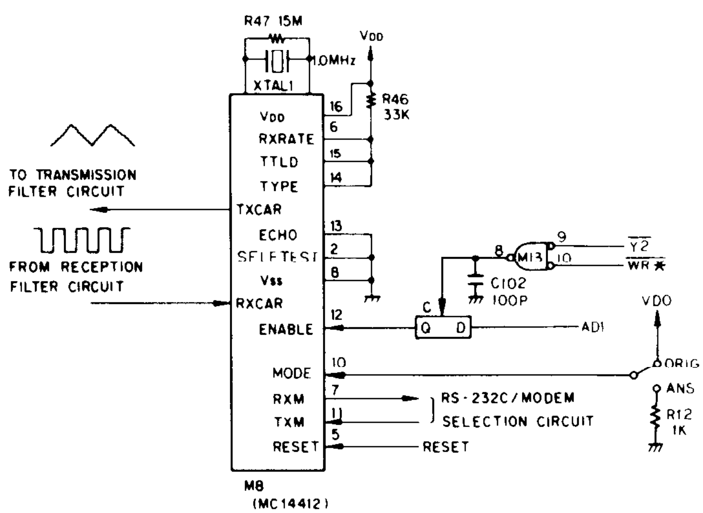


Figure 2-16. Modem IC and Peripheral Circuit

Transmission Filter Circuit

The transmit carrier signal output from the Tx terminal is DC by C61. The signal level is adjusted to -26.5 dB by variable resistor VR2. The signal then passes through the transmission band-pass filter and is sent to the telephone line or the acoustic coupler.

The transmission circuit is composed of an active filter (consisting of an operational amplifier) and the intermediate frequency, which changes according to the mode (originate or answer).

Depending on the ORIG/ANS switch setting, transistor (T4) is ON or OFF, so that R42 is 2.3 K Ohms for the answer mode, and the synthesis resistance of the R42 and R45 values determines the originate mode.

The intermediate frequency of the active filter is 1,170 Hz for the originate mode, and 2,125 Hz for the answer mode. See Figure 2-17.

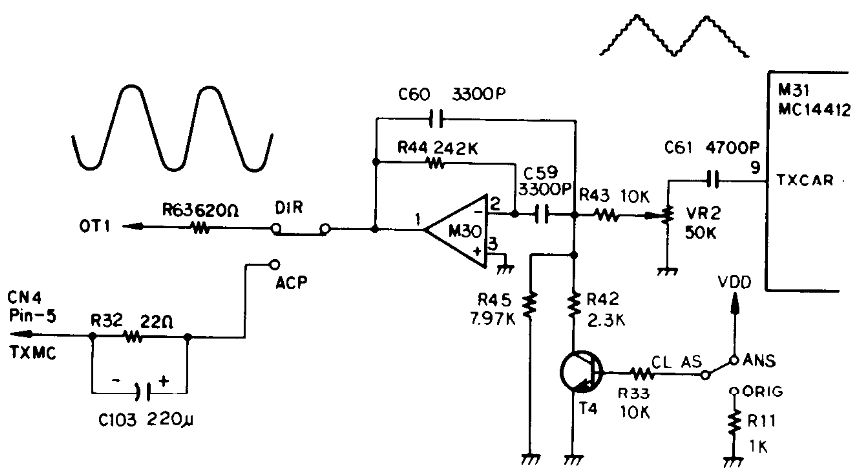


Figure 2-17. Transmission Filter Circuit

Reception Filter and Comparator Circuit

As shown in Figure 2-18, the reception circuit input signal is amplified when passing through the coupling capacitor, and amplified again as it passes through the 3-stage band-pass filter (composed of an active filter). The signal then passes through the comparator, and after being changed to a square-wave, is input at the RX CAR terminal of MC14412. Intermediate frequencies of the 3-stage active filter are also shown in figure 2-18.

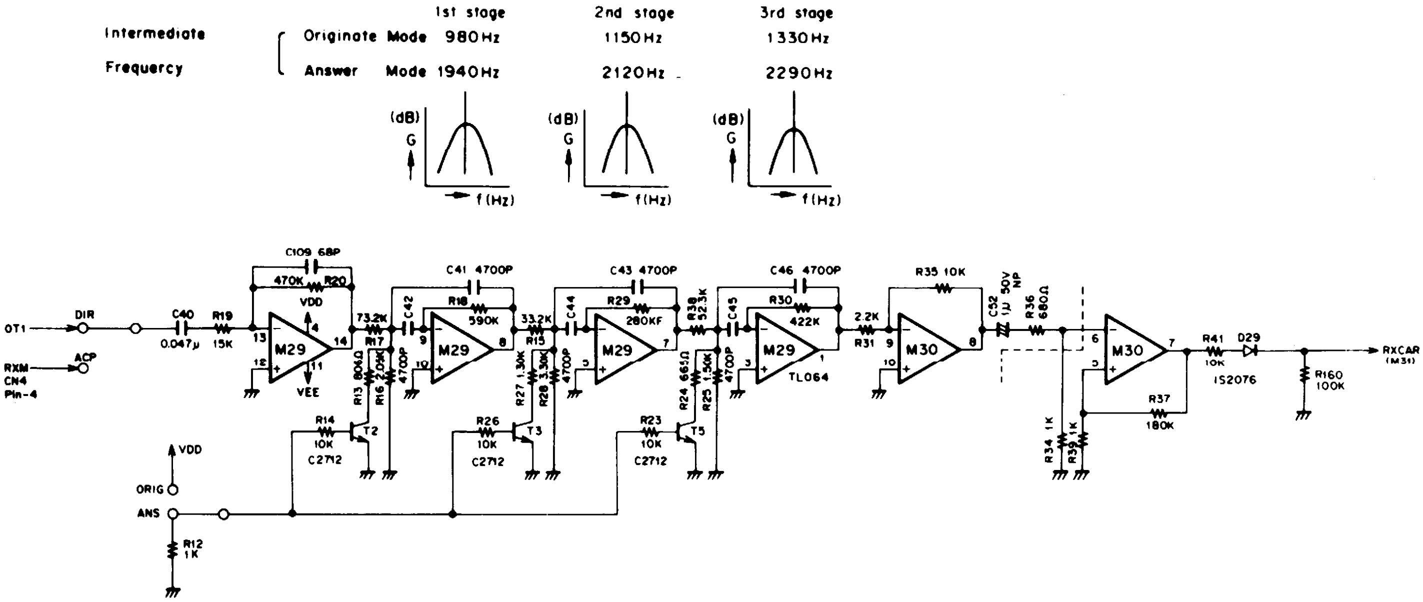


Figure 2-18. Reception Filter Circuit

Switching of the intermediate frequency for the Originate and Answer modes is accomplished by switching T2, T3, and T5 ON or OFF according to the ORIG/ANS switch setting, thus changing the value of the resistors.

Modem Connector Interface Circuit

When the acoustic coupler is used, transmission and reception signals are directly connected to the connector (TXM,RXM). When the modem cable is used (direct connection), transmission and reception signals are connected to the secondary side of the driver transformer. The primary side of this transformer is connected to the telephone line via the connector (TXMD, RXMD).

The ACP/DIR switch is used for selection of the acoustic coupler or the direct method of connection to the telephone lines.

When Tandy 102 is used in the terminal mode, relay RY3 separates the telephone receiver audio input signal (TL) to prevent interference. Relay RY2 separates the modem circuit and the telephone at the conclusion of use in the terminal mode and is also used as an automatic dialer.

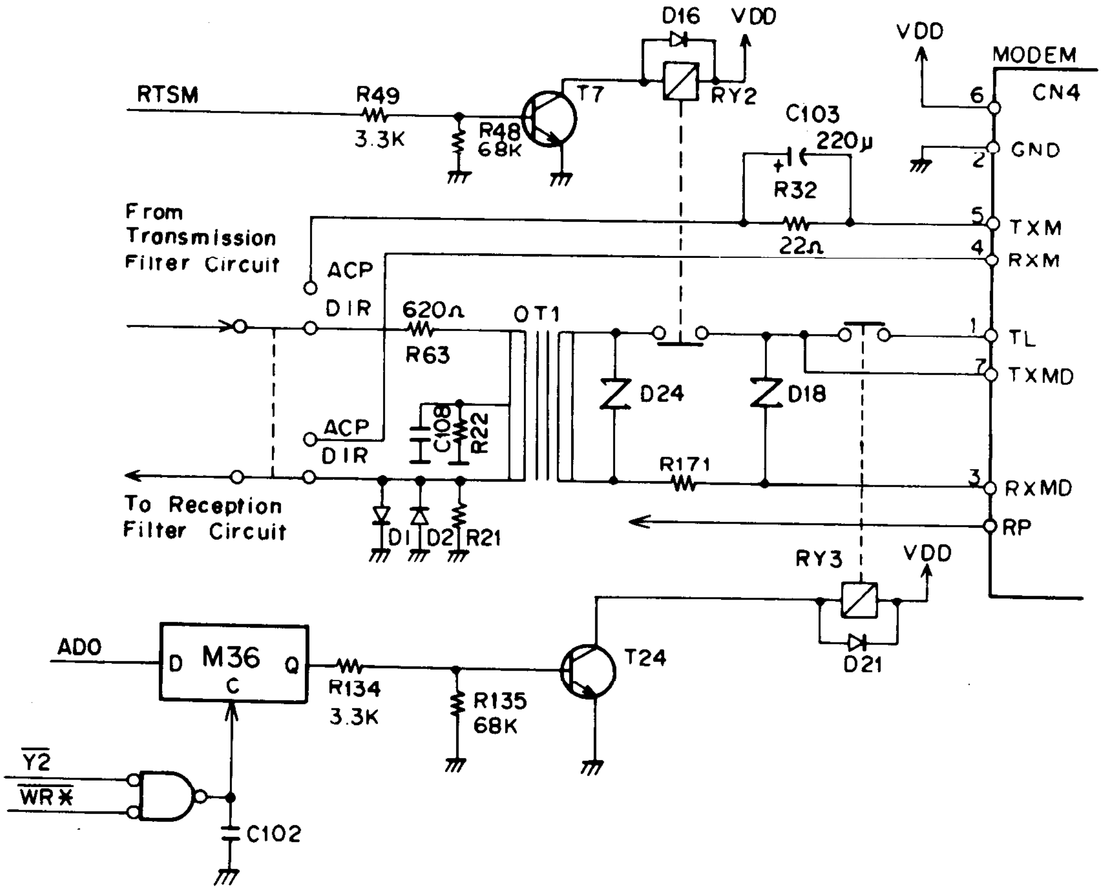


Figure 2-19. Modem Connector Interface Circuit

Liquid Crystal Display

The technical description of Tandy 102's liquid crystal display is divided into three sections:

- **LCD Panel**
- **LCD Control Circuit**
- **LCD Waveform**

LCD Panel

Liquid crystal is a substance midway between a liquid and a solid, although its appearance is much like a liquid. From an electrical and optical standpoint, it possesses the properties of a crystal. Items using this substance are called liquid crystal display elements. The LCD used in the Tandy 102 is a TN (Twisted Nematic) type of liquid crystal. Its basic construction is shown in Figure 2-20.

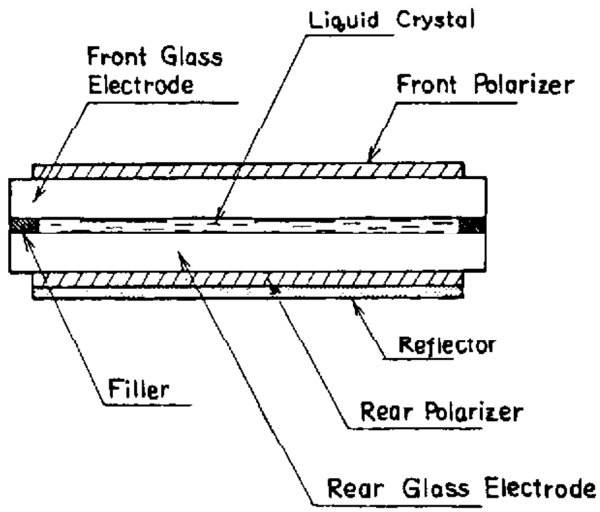


Figure 2-20. Construction of LCD Panel

The LCD operates as an "electric shutter" controlling the passage of light. That is, if voltage is applied, the transmission of light is blocked; otherwise light is allowed to pass.

Figure 2-21 demonstrates how the LCD operates:

1. The liquid-crystal display element is sandwiched between two polarization plates, with the polarized axes of the upper and lower plates positioned at right angles to each other.

2. As shown in Figure 2-21 (a), when the liquid is not electrically excited, its long cigar-shaped molecules are parallel to each other and perpendicular to the plates.

3. In Figure 2-21 (b), voltage is applied and the liquid appears frosted in current-carrying areas. Ion activity causes the molecules to scatter incident light.

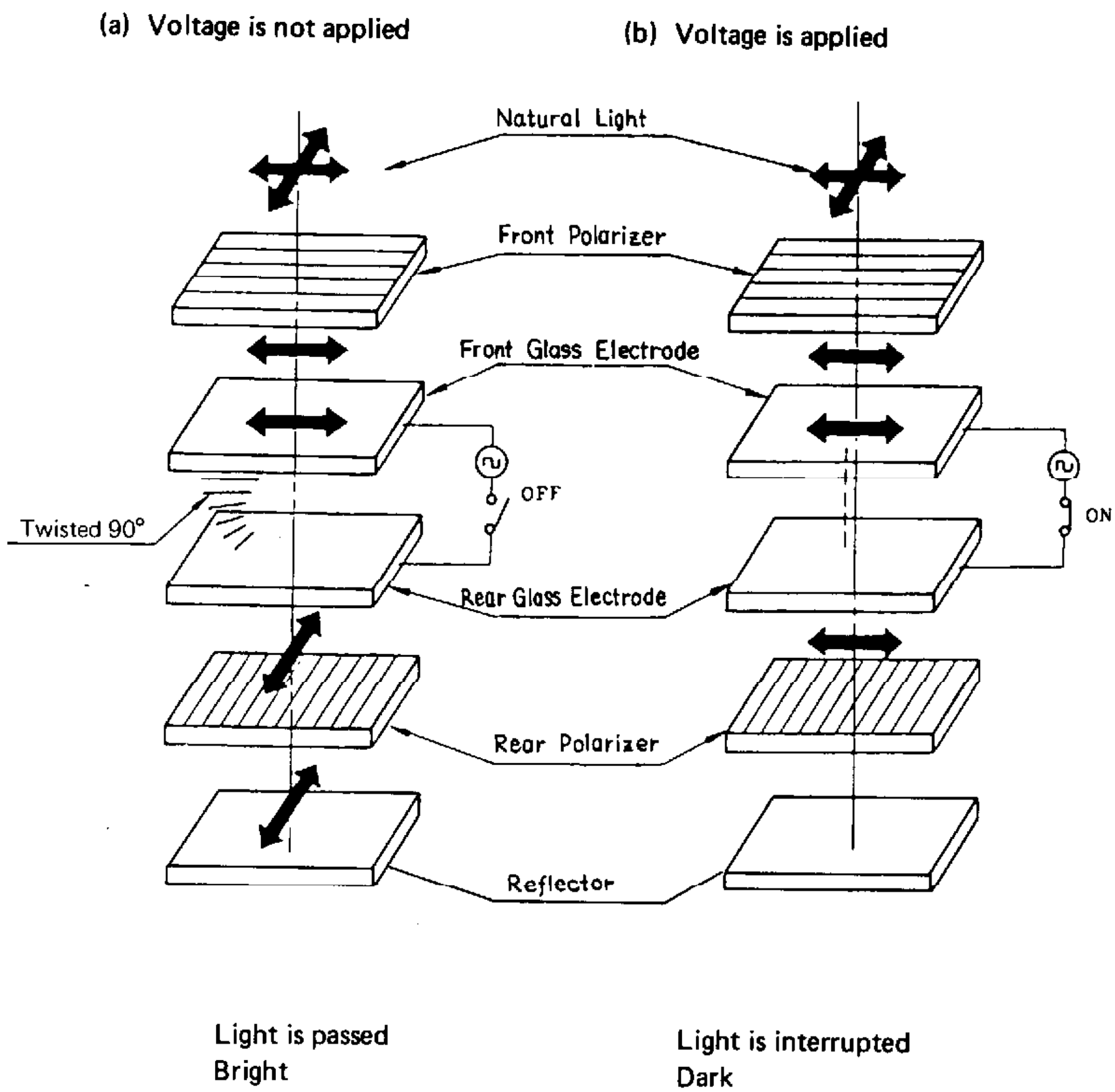


Figure 2-21. Operation Theory of LCD Panel

The LCD used in the Tandy 102 is composed of electrodes in a matrix arrangement (back scan 64, segments 480). Refer to Figure 2-22. Because the LCD operates on a 1/32 duty time-division drive, the upper 32 and lower 32 back scanning is performed by the same signal.

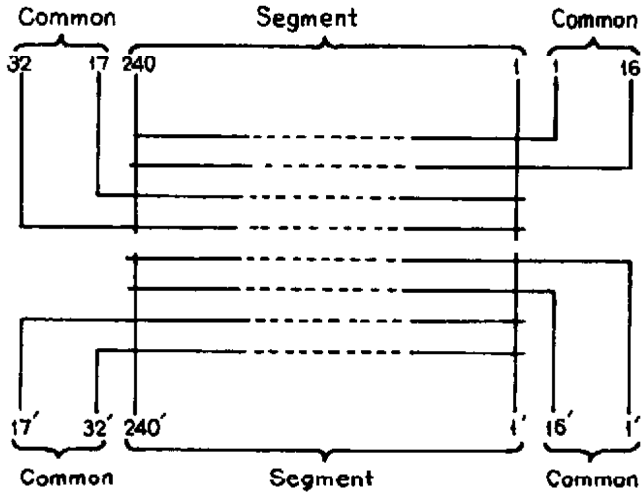


Figure 2-22. LCD Electrodes

The angle of the field of vision is 30° in the range that contrasts. K = 1.4 or more (brightness of non-illuminated segment divided by the brightness of illuminated segment). This range can be set by adjusting the LCD drive voltage with the Display Control Dial.

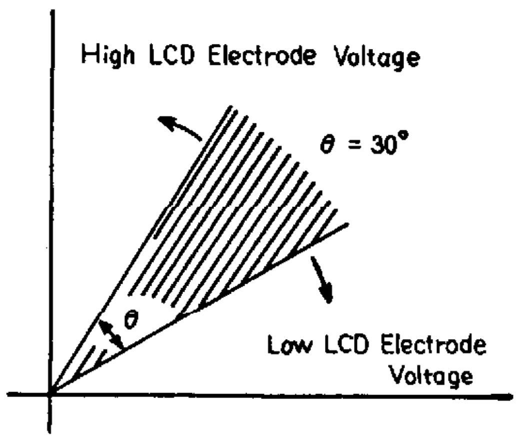


Figure 2-23. LCD View Angle

Caution: The polarization plate attached to the surface of the LCD panel is scratched very easily, and must be handled with great care.

To clean contacts or the display surface, dampen a soft cloth slightly with benzine and wipe gently. Do not use organic solvents such as alcohol.

LCD Control Circuit

Refer to the LCD PCB diagram, Figure 2-24, while reading this section.

ICs M11 and M12 (HD44103) are back-scan driver ICs. The timing signal necessary for the display is generated by the built-in oscillator, C5, and R10. This timing signal is also supplied to the segment driver for control of the display.

There are 16 HD44103 back-scan signal outputs. M11 and M12 are cascade connected, and a 1/32 duty back-scan signal is made. By using a capacitor and resistor only at the M11 side, a timing signal is generated which controls M12. M11 can then be considered as the master IC, and M12, the slave. The basic oscillation frequency is about 430kHz. Figure 2-24 shows the internal logic composition.

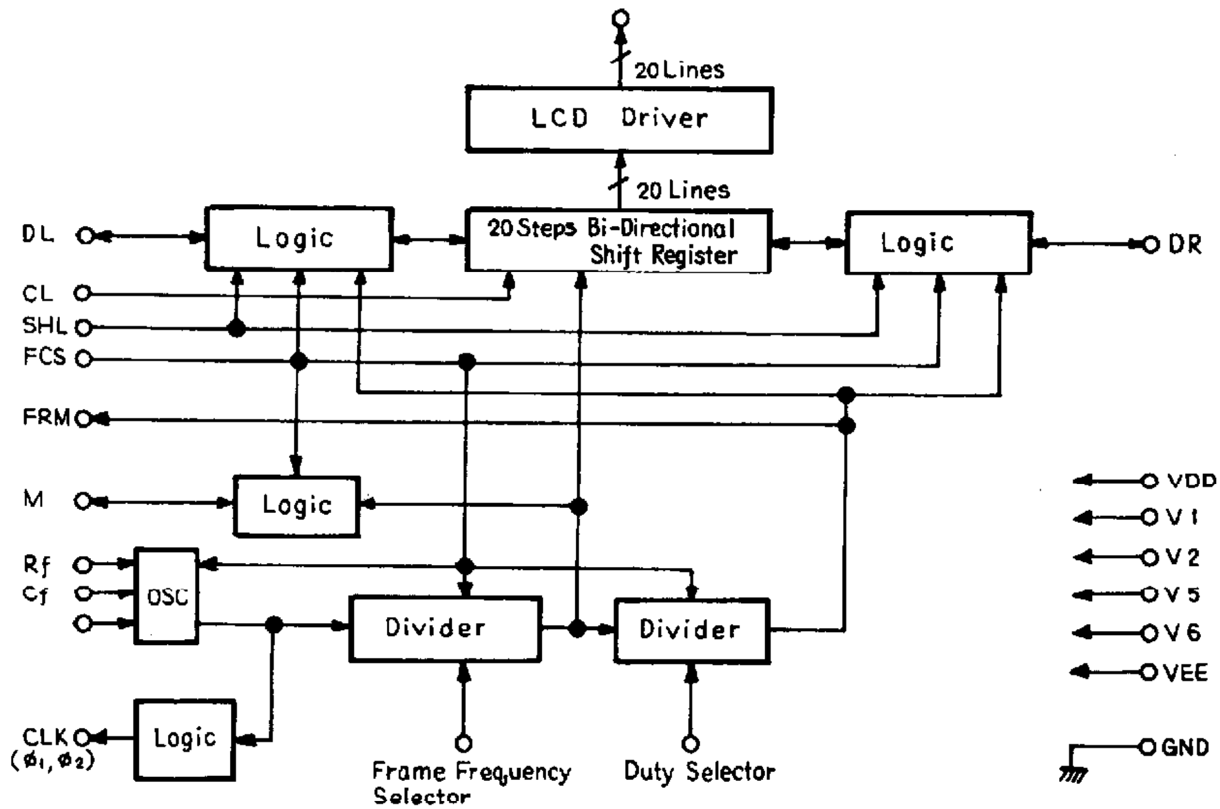


Figure 2-24. HD44103 Internal Logic Diagram

The timing signals are M, FRM, CLK (ϕ_1, ϕ_2), and CL. The M signal inverts the LCD drive waveform one image at a time to change it to AC. Since continuous application of DC to the LCD shortens the element life, an alternating electric field is applied to the liquid-crystal surface during drive to make the waveforms symmetrical and reduce the DC component.

The FRM signal is the display repeat frequency which sets the number of scans per second. For the Tandy 102, FRM $\simeq$ 70 Hz.

The ϕ_1 and ϕ_2 signals are the locks for HD44102 RAM operation.

The CL signal is the shift clock for the shift register.

ICs M1 - M10 (HD44102) are segment driver ICs that cause the display data sent from the CPU board to be memorized in the built-in RAM and automatically generate the liquid-crystal drive signal.

One bit of data from the built-in RAM corresponds to one dot of illumination or non-illumination on the display. The driver output is 50 lines. The transfer of the data is accomplished by 8-bit parallel data. This IC has several types of commands and the D/I (H: data, L: command) signal distinguishes between commands and data. Figure 2-25 shows the internal logic composition.

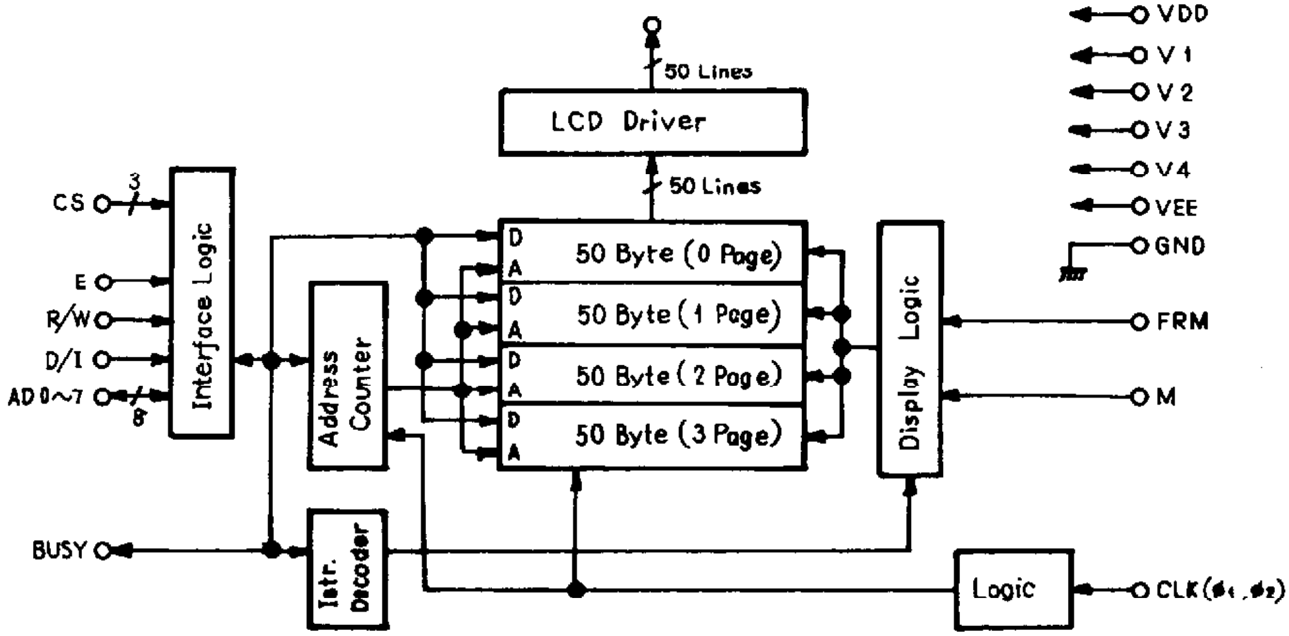


Figure 2-25. HD44102 Internal Logic Diagram

Because the Tandy 102 has 240 segments each (upper and lower), the M5 and M10 segment output Y41 - Y50 becomes NO-CONNECTION. The power supplied to these ICs, in addition to VDD (+5V) and VEE (−5V), includes V1 - V6.

VDD and VEE are the power supplies which operate the IC logic, and V1 - V6 make up the LCD signal. V1 - V6 are made up by the resistance splitting of R1, R2, R3, R4, and R5. By passing through operation amplifier M13 (LA6324), the output impedance of the power supply is lessened. Capacitors C3, C4, C6, C7, and C8 increase the peak current during LCD illumination. R11, R12, and R13 are resistors for 1C latch-up prevention.

This board also includes a low-power detection indicator and buzzer connectors.

LCD Waveform

To drive the liquid-crystal elements by the 1/32 duty line-sequential drive method, the LCD of the Tandy 102 makes sequential selection of the 32 scanning electrodes. For each dot, the display signal passes through the signal electrodes and is applied 32 times for one display. At this point, the signal is necessary at each dot only one time, and the signals for the other 31 times correspond to other dots on the same signal electrode.

The maximum voltage applied to the common electrode and segment electrode is the potential difference between V1 and V2.

In addition, **a** is the bias coefficient which determines, from the standpoint of contrast, the maximum ratio between the illumination and the non-illumination voltage.

When that ratio is greatest in relation to the effective ON and OFF voltages, **a** = 6.66. Thus, for V1, V2, V3, V4, V5, and V6:

V1 = VEE (−5V)
V2 = V (About 0 ~ 4V)
V3 = 2/aV
V4 = (1 - 2/a)V
V5 = (1 - 1/a)V
V6 = a/aV

Figure 2-26 shows the drive waveform for illumination and non-illumination.

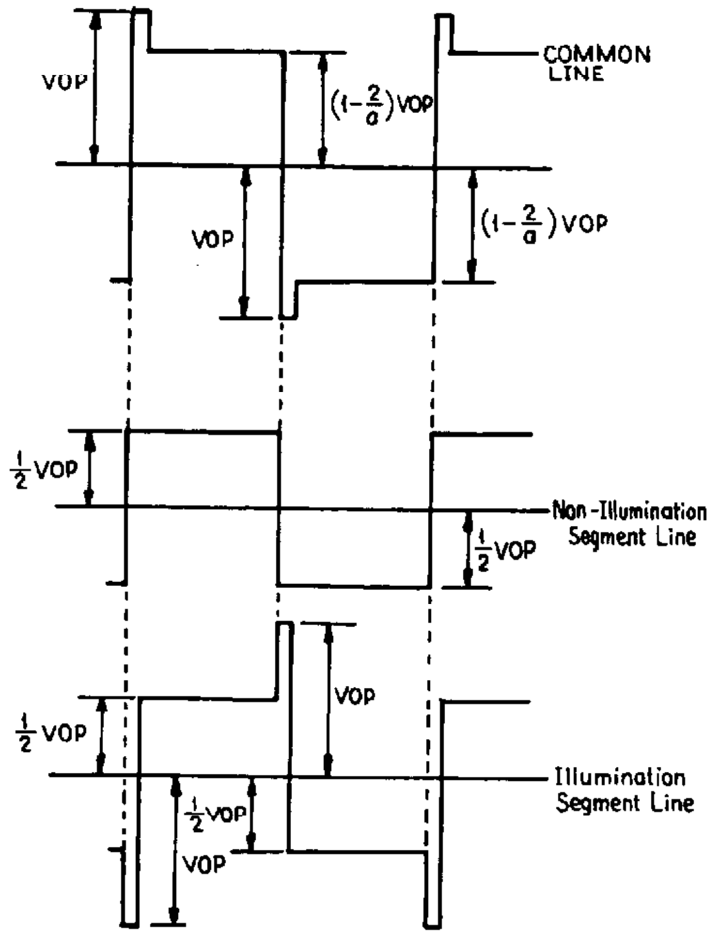


Figure 2-26. LCD Waveform

Power Supply and Automatic Power OFF Circuit

The power required by the logic circuits of Tandy 1Ø2 is ±5V, supplied by the DC/DC converter.

A special feature of the Tandy 1Ø2 is the Automatic Power OFF function. This circuit will be described in three parts; first, the circuit which supplies the power; secondly, the low-power detection and automatic power OFF circuits; and lastly, the reset circuit.

DC/DC Converter Circuit

OT2 is a converter transformer which oscillates T21 and T22 and generates voltage at the secondary side of the transformer. When the power is switched ON, a slight collector current flows to T21 and T22. A voltage between pins 7 and 9 of the converter transformer is generated, and the T22 base potential becomes positive. In other words, the base polarity becomes biased in the forward direction. This voltage causes the T21 and T22 base current to flow, and the collector current is increased.

When the collector current can no longer increase, because of transistor saturation resistance and converter coil resistance, the voltage between pins 7 and 9 begins to attenuate. As a result, the base current and collector current also attenuate, cutting off T21 and T22 due to the reverse bias action.

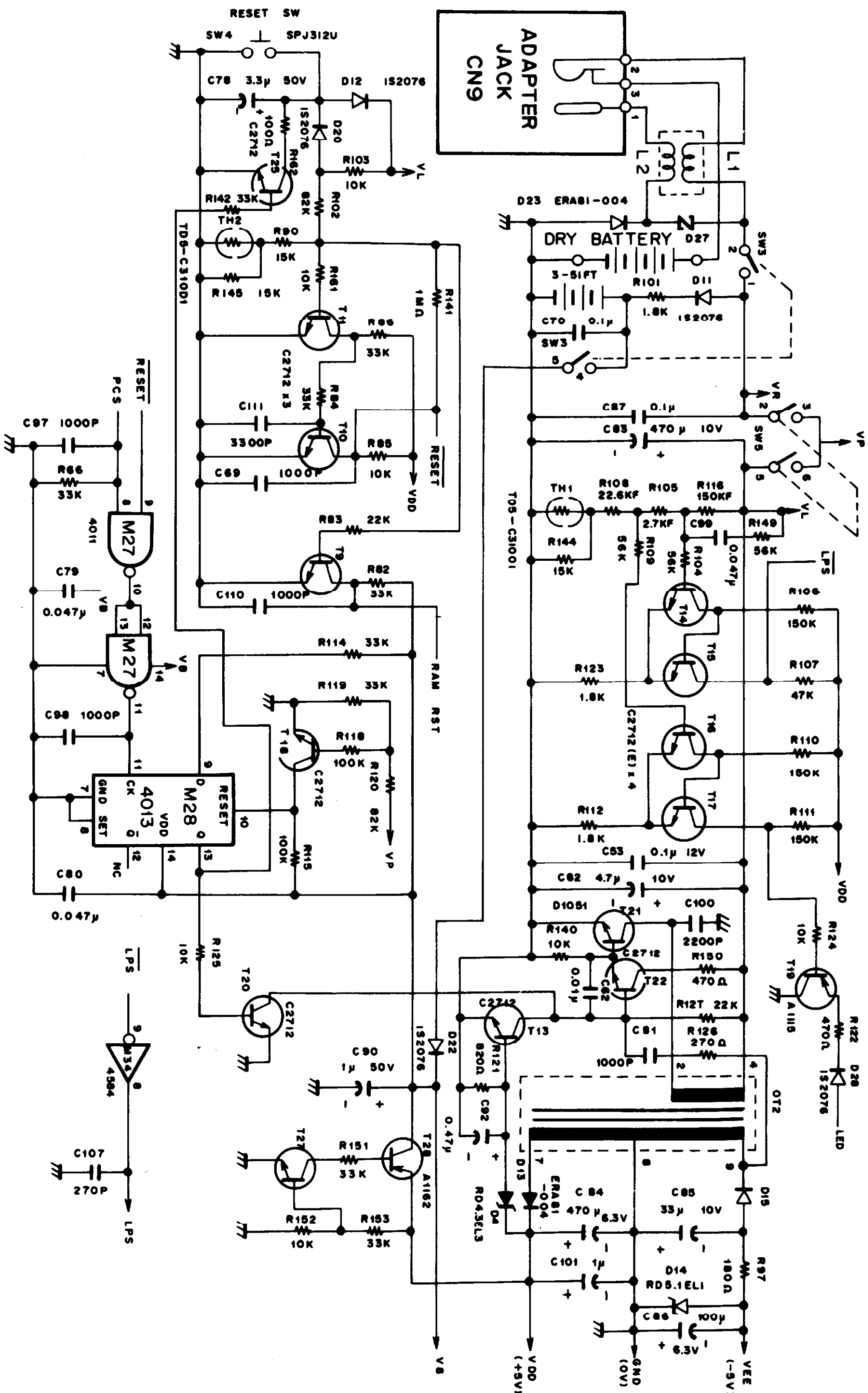


Figure 2-27. Power Supply and Reset Circuit

Until immediately before the transistor is cut off, an excitation current flows to the transformer. Since the current is suddenly cut off as a result of transistor cut-off, a counter voltage is generated, the distributed capacity of the coil is charged, and an oscillation voltage is generated at the base coil.

When the base potential reaches a half cycle of the oscillation voltage, it is biased in the forward direction and T21 and T22 are switched ON again.

In this way, AC voltage corresponding to the number of windings is generated at the secondary side of the converter. The voltage is rectified and smoothed by D13, D15, C84, and C85.

Voltage fluctuations of VDD (+5V) are fed back to the primary side of the oscillation transistor by T13, D4, R121, and C92 to improve stability. C81 and R126 make up a differentiation circuit designed to make the playback operation of the oscillation transistor easier. AC shorts the circuit so that the oscillation frequency is affected by the time-constant of this capacitor and resistor. Since feedback is applied by VDD (which makes stability difficult), VEE (−5V) is further stabilized by R97 and D14. (The voltage at both ends of C85 is about −7V). See Figure 2-27.

Low-Power Detection and Automatic Power OFF Circuit

The low-power detection circuit illuminates a warning indicator when the battery voltage decreases. If the voltage continues to decrease, the system power will switch off just before the voltage falls too low for the converter to operate. There will be about 20 minutes between the time the indicator illuminates and the system is switched off, provided there are no I/O devices connected.

Battery voltage is detected by splitting the resistance of R144, R108, R105, and R116. When battery voltage (VL) becomes 4.1V ±0.1V, T16 is switched off, T17 is switched on, T19 is driven, and the indicator illuminates. (The indicator is located on the LCD PCB.)

When VL becomes 3.7V ±0.1V, T14 is switched off, T15 is switched on, and LPS changes from H to L. This signal is inverted by M34 and fed to the TRAP terminal of 80C85. If the CPU acknowledges this signal, the P.C.S. signal is sent, passing through the PB4 of 81C55 after the internal operations.

The P.C.S. signal is active H. When P.C.S. becomes H, the Q output of M28 (4013: D type F/F) becomes H, T20 operates, and the oscillation of the converter is stopped.

If there is no operation for 10 minutes or more (awaiting a command for 10 minutes or more), P.C.S. is output from PB4 of 81C55.

When the power switch is switched OFF, T18 is switched OFF, the M28 RESET terminal becomes L and oscillation is resumed by turning the power switch ON. If the power is reduced by the LPS signal, battery replacement is necessary. R123 and R112 are resistors that provide hysteresis.

Reset Circuit

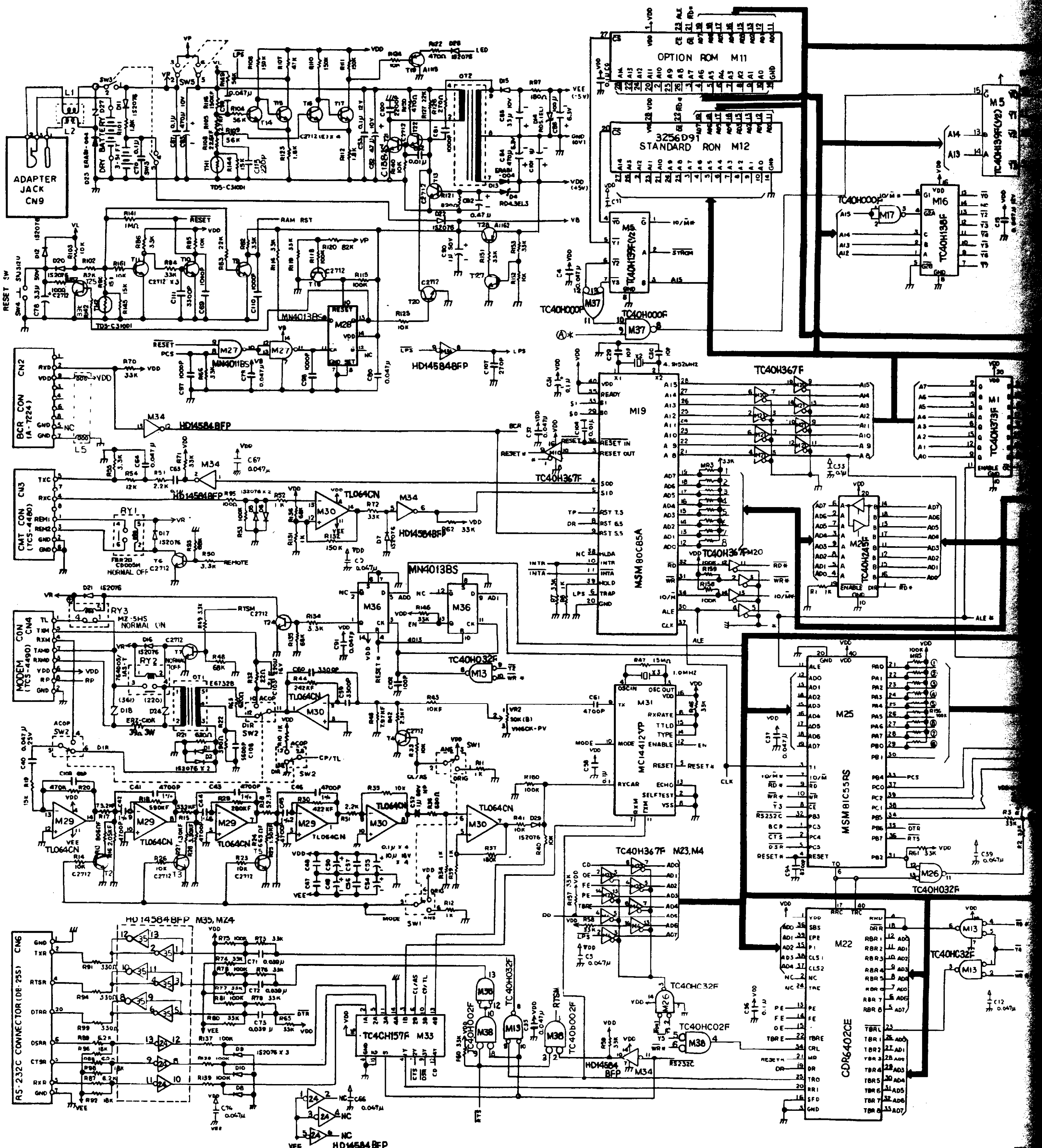
This curcuit supplies the CPU $\overline{\text{RESET}}$ signal and also the RAM RST signal as the RAM protecting signal when the power decreases. The circuit diagram is shown in Figure 2-27.

R103 and C78 delay the introduction of input power so that T11 is switched ON and T10 is switched OFF after VDD is activated. As a result, the $\overline{\text{RESET}}$ signal changes from L to H. The RAM RST signal is generated by T9 and changes from H to L.

R141 provides hysteresis to the $\overline{\text{RESET}}$ signal. Thermistor TH2 suppresses $\overline{\text{RESET}}$ signal fluctuations due to temperature. T25 receives the signal during automatic power-off, short-circuiting both ends of C78, and resets the system.

The $\overline{\text{RESET}}$ signal is active L and RAM RST signal is active H.

Section 3. Schematic Diagrams



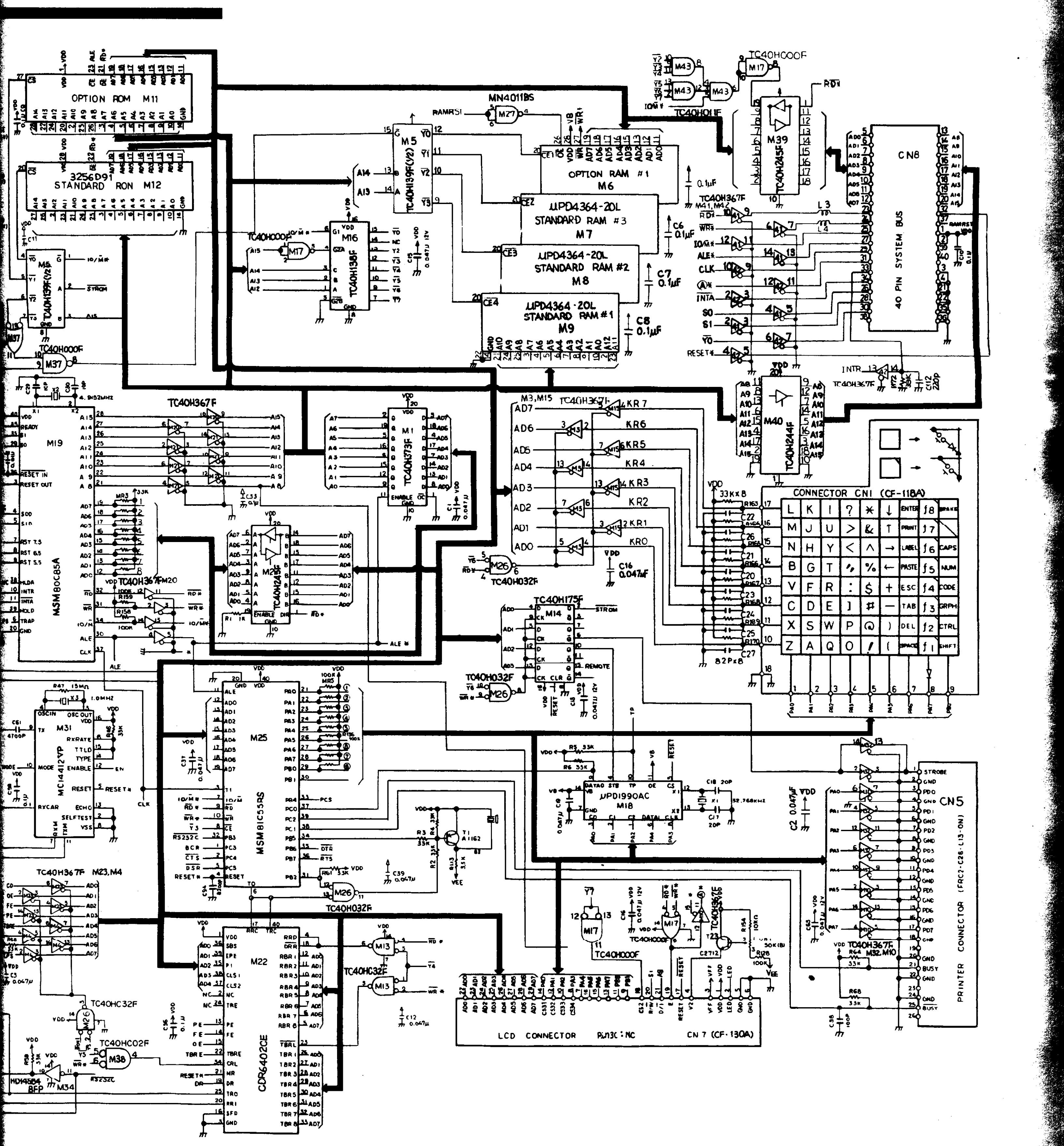
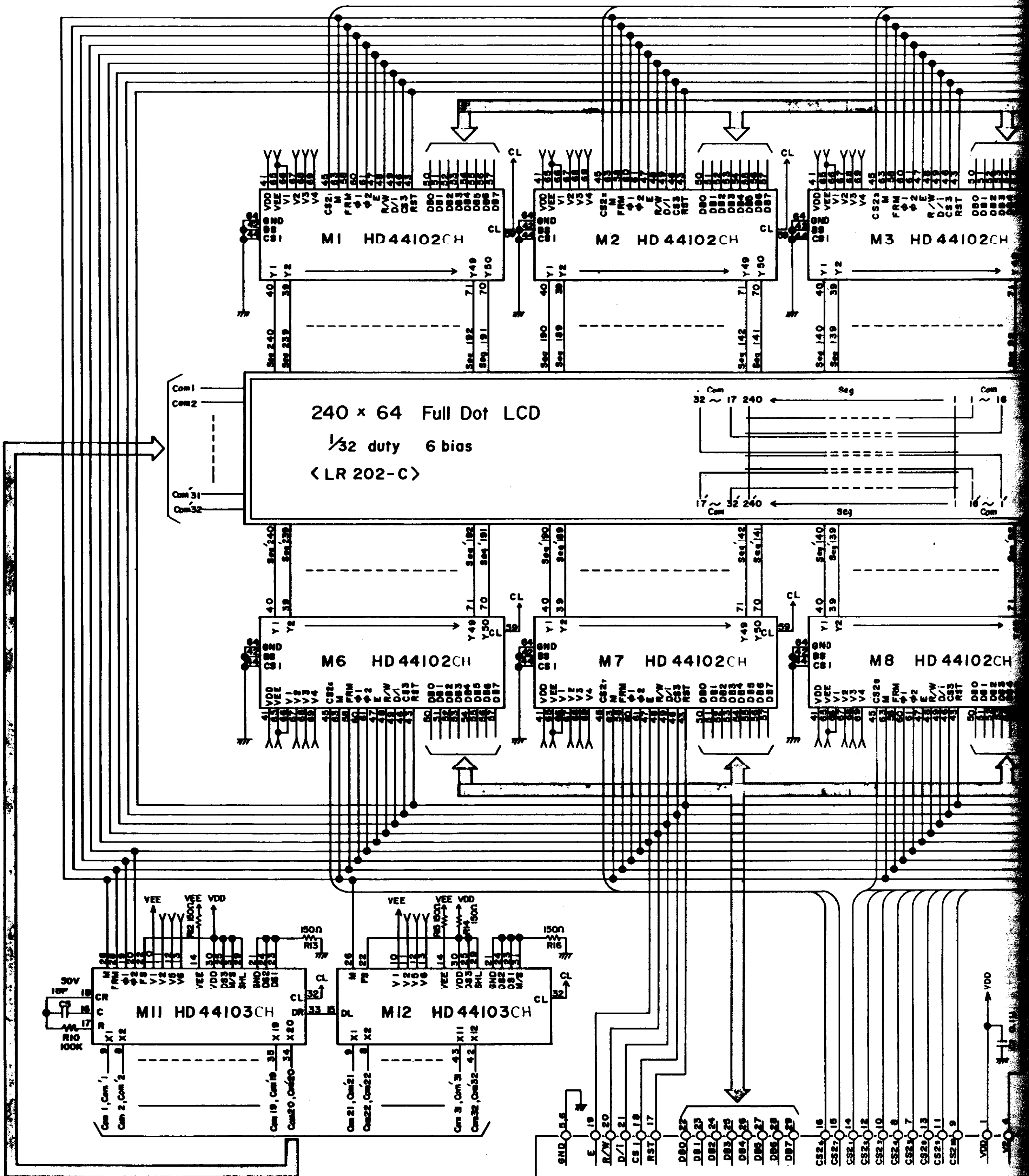


Figure 3-1. Main PCB — Schematic Diagram


240 × 64 Full Dot LCD
1/32 duty 6 bias
<LR 202-C>
M1 HD44102CH
M2 HD44102CH
M3 HD44102CH
M6 HD44102CH
M7 HD44102CH
M8 HD44102CH
M11 HD44103CH
M12 HD44103CH
Com1
Com2
Com31
Com32
CL
VEE
VDD
30V
150Ω
R13
R16
R10
100K
GND
E
R/W
D/I
CS1
RST
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
VDD

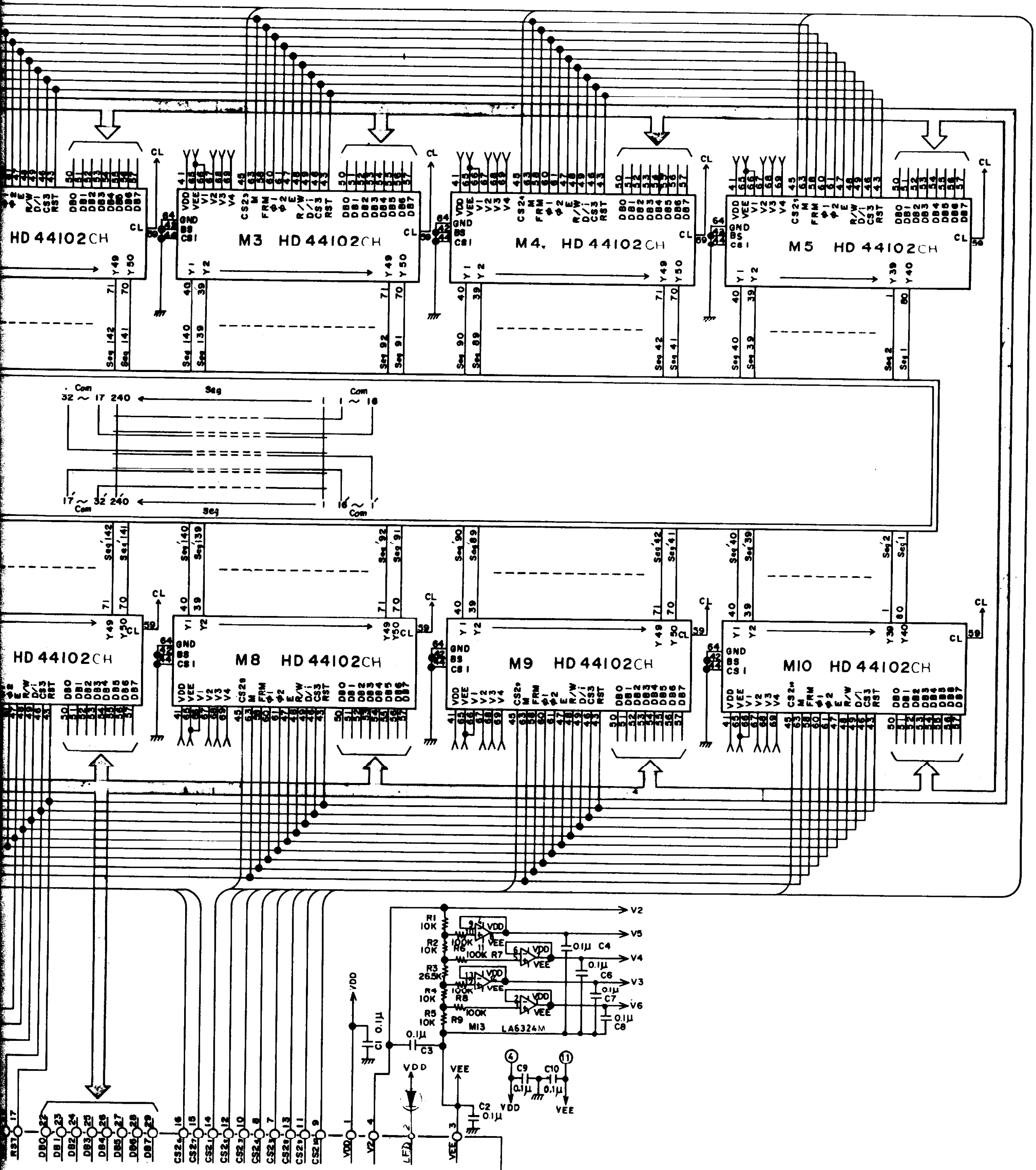


Figure 3-2. LCD PCB — Schematic Diagram

Section 4. ROM Subroutines

This section contains information on various ROM subroutines, including LCD, keyboard, printer, cassette recorder, RS-232C, and modem functions.

LCD Functions

LCD
Displays a character on the LCD at current cursor position.

Entry address (Hex): 4B44
Entry conditions: A = character to be displayed
Exit conditions: None

PLOT
Turns on pixel at specified location.

Entry address (Hex): 744C
Entry conditions: D = x coordinate (Ø-239)
E = y coordinate (Ø-63)
Exit conditions: None

UNPLOT
Turns off pixel at specified location.

Entry address (Hex): 744D
Entry conditions: D = x coordinate (Ø-239)
E = y coordinate (Ø-63)
Exit conditions: None

POSIT
Gets current cursor position.

Entry address (Hex): 427C
Entry condition: None
Exit conditions: H = column number (1-4Ø)
L = row number (1-8)

ESCA
Sends specified Escape Code Sequence.

Entry address (Hex): 4270
Entry conditions: A = escape code
Exit conditions: None

LCD Functions and Escape Codes

The routines for generating common LCD functions and escape codes have no entry or exit parameters.

Routine	Function	Entry Address (Hex)	Equiv. ESC
CRLF	Generates a carriage return and line feed	4222	—
HOME	Moves cursor to Home position (1,1)	422D	—
CLS	Clears display	4231	—
SETSYS	Sets system line (lock line 8)	4235	T
RSTSYS	Resets system line (unlock line 8)	423A	U
LOCK	Locks display (no scrolling)	423F	Y
UNLOCK	Unlocks display (scrolling)	4244	W
CURSON	Turns on cursor	4249	P
CUROFF	Turns off cursor	424E	Q
DELLIN	Deletes line at current cursor position	4253	M
INSLIN	Inserts a blank line at cursor position	4258	L
ERAEOL	Erases from cursor to end of line	425D	K
ENTREV	Sets reverse character mode	4269	p
EXTREV	Turns off reverse character mode	426E	q

LCD Variable and Status Locations

Name	Contents	Entry Address
CSRY	Cursor position (row)	F639
CSRX	Cursor position (column)	F63A
BEGLCD	Start of LCD memory	FE00
ENDLCD	End of LCD memory	FF40

Keyboard Functions

KYREAD
Scans keyboard for a key and returns with or without one.

Entry address (Hex): 7242
Entry conditions: None
Exit conditions: A = Character, if any

Z Flag: Set if no key found,
reset if key found
Carry: Set (character in code table below),
reset (normal character set code)

When Carry is set (1), Register A will contain one of the following:

Register A	Key Pressed
0	F1
1	F2
2	F3
3	F4
4	F5
5	F6
6	F7
7	F8
8	LABEL
9	PRINT
0A	SHIFT-PRINT
0B	PASTE

CHGET
Waits and gets character from keyboard.

Entry address (Hex): 12CB
Entry conditions: None
Exit conditions: A = character code
Carry: Set if special character,
reset if normal character
((F1) - (F8) return preprogrammed strings)

CHSNS
Checks keyboard queue for characters.

Entry address (Hex): 13DB
Entry conditions: None
Exit conditions: Z flag: Set if queue empty,
reset if keys pending

KEYX
Checks keyboard queue for characters or BREAK.

Entry address (Hex): 7270
Entry conditions: None
Exit conditions: Z flag set if queue empty,
reset if keys pending
Carry: Set when BREAK entered,
reset with any other key

BRKCHK
Checks for BREAK characters only (CTRL C or CTRL S).

Entry address (Hex): 7283
Entry conditions: None
Exit conditions:
Carry: Set if BREAK or PAUSE entered,
reset if no BREAK characters

INLIN
Gets line from keyboard. Terminated by (ENTER).

Entry address (Hex): 4644
Entry conditions: None
Exit conditions: Data stored at location F685

Using Function Key Routines

The function table consists of character strings to be used by the keyboard driver when processing (F1) - (F8) keys. The strings have a maximum length of 16 characters and are terminated by an 80 (hex) code. If the last character of the string is ORed with 80, the character will also serve as a terminator. The entire string will be placed in the keyboard buffer when the appropriate function key is pressed. You must specify character strings for all 8 function keys. (Use the terminator byte for any string you wish to ignore.)

Example of function table:

```
FCTAB   DEFM   'Files'   ; F1
        DEFW   0D80
        DEFM   'Load'    ; F2
        DEFB   80
        DEFM   'Save'    ; F3
        DEFB   80
        DEFM   'Run'     ; F4
        DEFW   0D80
        DEFM   'List'    ; F5
        DEFW   0D80
        DEFB   80        ; Ignore F6
        DEFB   80        ; Ignore F7
        DEFM   'Menu'    ; F8
        DEFW   0D80
```

STFNK
Sets function key definitions.

Entry address (Hex): 5A7C
Entry conditions:
HL = Address of function table (above)
Exit conditions: None

CLRFLK
Clears function key definition table (fills table with 80s).

Entry address (Hex): 5A79
Entry conditions: None
Exit conditions: None

DSPFNK
Displays function keys.

Entry address (Hex): 42A8
Entry conditions: None
Exit conditions: None

STDSPF
Sets and displays function keys.

Entry address (Hex): 42A5
Entry conditions:
HL = Start address of function table
Exit conditions: None

ERAFNK
Erases function key display.

Entry address (Hex): 428A
Entry conditions: None
Exit conditions: None

FNKSB
Displays function table (if enabled).

Entry address (Hex): 5A9E
Entry conditions: None
Exit conditions: None

Printing Routines

PRINTR
Sends a character to the line printer.

Entry address (Hex): 6D3F
Entry conditions: A = character to be printed
Exit conditions:
Carry: Set if cancelled by BREAK,
reset if normal return

PNOTAB
Prints character without expanding tab characters.

Entry address (Hex): 1470
Entry conditions: A = character to be printed
Exit conditions: Unknown

PRTTAB
Prints a character expanding tabs to spaces.

Entry address (Hex): 4B55
Entry conditions: A = character to be printed
Exit conditions: Unknown

PRTLCD
Prints contents of LCD.

Entry address (Hex): 1E5E
Entry conditions: None
Exit conditions: None

RS-232C and Modem Routines

DISC
Disconnects phone line.

Entry address (Hex): 52BB
Entry conditions: None
Exit conditions: None

CONN
Connects phone line.

Entry address (Hex): 52D0
Entry conditions: None
Exit conditions: None

DIAL
Dials a specified phone number.

Entry address (Hex): 532D
Entry conditions: HL = phone number address
Exit conditions: None

RCVX
Checks RS-232 queue for characters.

Entry address (Hex): 6D6D
Entry conditions: None
Exit conditions: A = number of characters queue
Z flag: Set if no data, reset if characters pending

RV232C
Gets a character from RS-232 receive queue.

Entry address (Hex): 6D7E
Entry conditions: None
Exit conditions: A = character received
Z flag: Set if O.K., reset if error (PE, FF, or OF)
Carry: Set if BREAK pressed, else reset

SENDCQ
Sends an XON resume character (CTRL Q).

Entry address (Hex): 6E0B
Entry conditions: None
Exit conditions: None

SENDCS
Sends an XOFF pause character (CTRL S).

Entry address (Hex): 6E1E
Entry conditions: None
Exit conditions: None

SD232C
Sends a character to the RS-232 or modem (with XON/XOFF).

Entry address (Hex): 6E32
Entry conditions: A = character to be sent
Exit conditions: Unknown

CARDET
Detects carrier (for modem only).

Entry address (Hex): 6EEF
Entry conditions: None
Exit conditions: A = Ø if carrier
Z Flag: Set if carrier, else reset

BAUDST
Sets baud rate for RS-232C.

Entry address (Hex): 6E75
Entry conditions: H = Baud rate (1-9,M)
Exit conditions: None

INZCOM
Initializes RS-232C and modem.

Entry address (Hex): 6EA6
Entry conditions:
H = Baud rate (1-9, M)
L = UART configuration code
(See UART byte description below)
Carry: Set if RS-232C, reset if modem
Exit conditions: None

Bits(s)	Description	
0	Number of Stop Bits	: 0=1, 1=2
1	Parity setting	: 0 = Odd 1 = Even
2	Parity disable	: 0 = Enable 1 = Disable
3-4	Word length	: 01 = 6, 10 = 7, 11 = 8

The byte is ANDed with 1FH to ignore bits 5-7. The text string containing the current STAT setting is located at F65BH (5 bytes): baud, length, parity, stop bits, and XON/XOFF switch.

SETSER
Sets serial interface parameters. Activates RS-232C/Modem.

Entry address (Hex): 17E6
Entry conditions: HL = start address of ASCII string containing parameter terminated by zero (78E1E, Ø).
Syntax same as in Telcom's STAT
Carry: Set for RS-232C, reset for modem
Exit conditions: None

CLSCOM
Deactivates RS-232C/Modem.

Entry address (Hex): 6ECB
Entry conditions: None
Exit conditions: None

Cassette Recorder Routines

DATAR
Reads character from cassette (no checksum).

Entry address (Hex): 702A
Entry conditions: None
Exit conditions: D = character from cassette

CTON
Turns on motor.

Entry address (Hex): 14A8
Entry conditions: None
Exit conditions: None

CTOFF
Turns off motor.

Entry address (Hex): 14AA
Entry conditions: None
Exit conditions: None

CASIN
Reads a character from cassette and updates checksum.

Entry address (Hex): 14B0
Entry conditions: C = current checksum
Exit conditions: A = character
C = contains the updated checksum

CSOUT
Sends character to cassette and updates checksum.

Entry address (Hex): 14C1
Entry conditions: A = character to be sent
C = current checksum
Exit conditions: C = updated checksum

SYNCW
Writes cassette header and sync byte only.

Entry address (Hex): 6F46
Entry conditions: None
Exit conditions: None

SYNCR
Reads cassette header and sync byte only.

Entry address (Hex): 6F85
Entry conditions: None
Exit conditions: None

DATAW
Writes a character to cassette (no checksum).

Entry address (Hex): 6F5B
Entry conditions: A = character to be sent
Exit conditions: None

RAM File Routines

The directory table (F962) contains information on all file location, type, and status.

Each file is managed by an 11-byte directory entry in the format:

Byte 1	:	Directory Flag (for file type and status)
Bytes 2-3	:	Address of file
Bytes 4-11	:	8-byte filename

The Directory Flag contains the following information:

Bit 7 (MSB)	1 if a valid entry
Bit 6	1 for ASCII text file (DO)
Bit 5	1 for machine language (CO)
Bit 4	1 for ROM file
Bit 3	1 for invisible file
Bit 2	reserved for future use
Bit 1	reserved for future use
Bit 0	internal use only

MAKTXT
Creates a text file.

Entry address (Hex): 22Ø F
Entry conditions: Filename (max. 8 bytes) must be stored in FILNAM (FC93). 'DO' extension not required
Exit conditions: HL = TOP address of new file
DE = address of Directory entry (Flag)
Carry: Set if file already exists
Reset if new file

CHKDC
Searches for file in directory.

Entry address (Hex): 5AA9
Entry conditions: DE = address of filename to find (ASCII filename + Ø byte terminator)
Exit conditions: HL = start address (TOP) of file
Z Flag: Ø (file found)
1 (file not found)

GTXTTB
Gets top address of file.

Entry address (Hex): 5AE3
Entry conditions: HL = address of directory entry for file
Exit conditions: HL = TOP start address of file

KILASC
Kills a text (DO) file.

Entry address (Hex): 1FBE
Entry conditions: DE = file TOP start address
HL = address of directory entry (flag)
Exit conditions: None

INSCHR
Inserts a character in a file.

Entry address (Hex): 6B61
Entry conditions: A = character to insert
HL = address to insert character
Exit conditions: HL = HL + 1
Carry: Set if out of memory

MAKHOL
Inserts a specified number of spaces in a file.

Entry address (Hex): 6B6D
Entry conditions: BC = number of spaces to insert
HL = address to insert spaces
Exit conditions: HL and BC are preserved
Carry: Set if out of memory

MASDEL
Deletes specified number of characters.

Entry address (Hex): 6B9F
Entry conditions: BC = number of characters to delete
HL = address of deletion
Exit conditions: HL and BC are preserved

Other Routines

INITIO
Cold start reset.

Entry address (Hex): 6CD6
Entry conditions: None
Exit conditions: None

IOINIT
Warm start reset.

Entry address (Hex): 6CE0 27872
Entry conditions: None
Exit conditions: None

MENU
Goes to Main Menu.

Entry address (Hex): 5797
Entry conditions: None
Exit conditions: None

MUSIC
Makes tone.

Entry address (Hex): 72C5
Entry conditions: DE = frequency (See the Tandy 102 Owner's Manual, Cat. No. 26-3803)
B = duration (See the Tandy 102 Owner's Manual, Cat. No. 26-3803)
Exit conditions: None

TIME
Reads system TIME.

Entry address (Hex): 190F
Entry conditions: HL = address of 8-byte area for TIME
Exit conditions: HL → TIME (hh:mm:ss)

DATE
Reads system DATE.

Entry address (Hex): 192F
Entry conditions: HL = address of 8-byte area for DATE
Exit conditions: HL → DATE (mm/dd/yy)

DAY
Reads system DAY of the week.

Entry address (Hex): 1962
Entry conditions: HL = address of 3-byte area for DAY
Exit conditions: HL → DAY (ddd)

Section 5. Character Code Table

ASCII Character Code Tables

Decimal	Hex	Binary	Printed Character	Keyboard Character
0	00	00000000		CTRL @
1	01	00000001		CTRL A
2	02	00000010		CTRL B
3	03	00000011		CTRL C
4	04	00000100		CTRL D
5	05	00000101		CTRL E
6	06	00000110		CTRL F
7	07	00000111		CTRL G
8	08	00001000		CTRL H
9	09	00001001		CTRL I
10	0A	00001010		CTRL J
11	0B	00001011		CTRL K
12	0C	00001100		CTRL L
13	0D	00001101		CTRL M
14	0E	00001110		CTRL N
15	0F	00001111		CTRL O
16	10	00010000		CTRL P
17	11	00010001		CTRL Q
18	12	00010010		CTRL R
19	13	00010011		CTRL S
20	14	00010100		CTRL T
21	15	00010101		CTRL U
22	16	00010110		CTRL V
23	17	00010111		CTRL W
24	18	00011000		CTRL X
25	19	00011001		CTRL Y
26	1A	00011010		CTRL Z
27	1B	00011011		ESC
28	1C	00011100		→
29	1D	00011101		←
30	1E	00011110		↑
31	1F	00011111		↓
32	20	00100000		SPACEBAR
33	21	00100001	!	!
34	22	00100010	"	"
35	23	00100011	#	#
36	24	00100100	$	$
37	25	00100101	%	%
38	26	00100110	&	&
39	27	00100111	'	'
40	28	00101000	(	(
41	29	00101001	)	)
42	2A	00101010	*	*
43	2B	00101011	+	+
44	2C	00101100	,	,
45	2D	00101101	–	–
46	2E	00101110		.
47	2F	00101111	/	/
48	30	00110000	0	0
49	31	00110001	1	1
50	32	00110010	2	2
51	33	00110011	3	3
52	34	00110100	4	4
53	35	00110101	5	5
54	36	00110110	6	6
55	37	00110111	7	7
56	38	00111000	8	8
57	39	00111001	9	9
58	3A	00111010	:	:
59	3B	00111011	;	;
60	3C	00111100	<	<
61	3D	00111101	=	=
62	3E	00111110	>	>
63	3F	00111111	?	?
64	40	01000000	@	@
65	41	01000001	A	A
66	42	01000010	B	B
67	43	01000011	C	C
68	44	01000100	D	D
69	45	01000101	E	E
70	46	01000110	F	F

* For uppercase letters A-Z, press SHIFT or CAPS LOCK before pressing the Keyboard Character.

Decimal	Hex	Binary	Printed Character	Keyboard Character
71	47	01000111	G	G
72	48	01001000	H	H
73	49	01001001	I	I
74	4A	01001010	J	J
75	4B	01001011	K	K
76	4C	01001100	L	L
77	4D	01001101	M	M
78	4E	01001110	N	N
79	4F	01001111	O	O
80	50	01010000	P	P
81	51	01010001	Q	Q
82	52	01010010	R	R
83	53	01010011	S	S
84	54	01010100	T	T
85	55	01010101	U	U
86	56	01010110	V	V
87	57	01010111	W	W
88	58	01011000	X	X
89	59	01011001	Y	Y
90	5A	01011010	Z	Z
91	5B	01011011	[	[
92	5C	01011100	\	GRPH -
93	5D	01011101	]	]
94	5E	01011110	^	^
95	5F	01011111	_	_
96	60	01100000	\`	GRAPH |
97	61	01100001	a	A
98	62	01100010	b	B
99	63	01100011	c	C
100	64	01100100	d	D
101	65	01100101	e	E
102	66	01100110	f	F
103	67	01100111	g	G
104	68	01101000	h	H
105	69	01101001	i	I
106	6A	01101010	j	J
107	6B	01101011	k	K
108	6C	01101100	l	L
109	6D	01101101	m	M
110	6E	01101110	n	N
111	6F	01101111	o	O
112	70	01110000	p	P
113	71	01110001	q	Q
114	72	01110010	r	R
115	73	01110011	s	S
116	74	01110100	t	T
117	75	01110101	u	U
118	76	01110110	v	V
119	77	01110111	w	W
120	78	01111000	x	X
121	79	01111001	y	Y
122	7A	01111010	z	Z

* For lowercase letters a-z, be sure CAPS LOCK is not pressed "down."

Decimal	Hex	Binary	Printed Character	Keyboard Character
123	7B	01111011	{	GRPH 9
124	7C	01111100	|	GRPH _
125	7D	01111101	}	GRPH 0
126	7E	01111110	~	GRPH]
127	7F	01111111		DEL
128	80	10000000	☎	GRPH p
129	81	10000001		GRPH m
130	82	10000010		GRPH f
131	83	10000011		GRPH x
132	84	10000100		GRPH c
133	85	10000101	✝	GRPH a
134	86	10000110		GRPH h
135	87	10000111		GRPH t
136	88	10001000	i	GRPH l
137	89	10001001	\ ‾	GRPH r
138	8A	10001010	≠	GRPH /
139	8B	10001011	Σ	GRPH s
140	8C	10001100	≈	GRPH '
141	8D	10001101	±	GRPH =
142	BE	10001110	∫	GRPH i
143	BF	10001111	◀	GRPH e
144	90	10010000		GRPH y
145	91	10010001		GRPH u
146	92	10010010	↕	GRPH ;
147	93	10010011		GRPH q
148	94	10010100		GRPH w
149	95	10010101	♂	GRPH b
150	96	10010110	♀	GRPH n
151	97	10010111	℅	GRPH .
152	98	10011000	↑	GRPH o
153	99	10011001	↓	GRPH ,
154	9A	10011010	→	GRPH j
155	9B	10011011	←	GRPH k
156	9C	10011100	♧	GRPH 2
157	9D	10011101	♢	GRPH 3
158	9E	10011110	♡	GRPH 4
159	9F	10011111	♤	GRPH 5
160	A0	10100000	´	CODE '
161	A1	10100001	a	CODE x
162	A2	10100010	ç	CODE c
163	A3	10100011	£	GRPH 8
164	A4	10100100	·	CODE "
165	A5	10100101	µ	CODE M
166	A6	10100110	°	CODE)
167	A7	10100111	▼	CODE _
168	A8	10101000	†	CODE +
169	A9	10101001		CODE s
170	AA	10101010		CODE R
171	AB	10101011		CODE C
172	AC	10101100	¼	CODE p
173	AD	10101101	¾	CODE ;
174	AE	10101110	½	CODE /
175	AF	10101111	‹	CODE 0

Decimal	Hex	Binary	Printed Character	Keyboard Character
176	B0	10110000	¥	GRPH 7
177	B1	10110001	Ä	CODE A
178	B2	10110010	Ö	CODE O
179	B3	10110011	Ü	CODE U
180	B4	10110100	¢	GRPH 6
181	B5	10110101	-	CODE [
182	B6	10110110	ä	CODE a
183	B7	10110111	ö	CODE o
184	B8	10111000	ü	CODE u
185	B9	10111001	B	CODE S
186	BA	10111010	ᵀᴹ	CODE T
187	BB	10111011	é	CODE d
188	BC	10111100	ù	CODE ,
189	BD	10111101	è	CODE v
190	BE	10111110	¨	CODE =
191	BF	10111111	£	CODE F
192	C0	11000000	â	CODE !
193	CI	11000001	ê	CODE 3
194	C2	11000010	î	CODE 8
195	C3	11000011	ô	CODE 9
196	C4	11000100	û	CODE 7
197	C5	11000101	-	CODE –
198	C6	11000110	ë	CODE e
199	C7	11000111	ï	CODE i
200	C8	11001000	á	CODE q
201	C9	11001001	í	CODE k
202	CA	11001010	ó	CODE l
203	CB	11001011	ú	CODE j
204	CC	11001100	ý	CODE y
205	CD	11001101	ñ	CODE n
206	CE	11001110	ã	CODE z
207	CF	11001111	õ	CODE
208	D0	11010000	Â	CODE !
209	D1	11010001	Ê	CODE #
210	D2	11010010	Î	CODE *
211	D3	11010011	Ô	CODE (
212	D4	11010100	Û	CODE &
213	D5	11010101	Ï	CODE l
214	D6	11010110	Ë	CODE E
215	D7	11010111	É	CODE D
216	D8	11011000	Á	CODE Q
217	D9	11011001	Í	CODE K
218	DA	11011010	Ó	CODE L
219	DB	11011011	Ú	CODE J
220	DC	11011100	Ý	CODE Y
221	DD	11011101	Ù	CODE <
222	DE	11011110	È	CODE V
223	DF	11011111	À	CODE X
224	ED	11100000		GRPH Z
225	E1	11100001	▘ (upper left)	GRPH !
226	E2	11100010	▝ (upper right)	GRPH @
227	E3	11100011	▖ (lower left)	GRPH #
228	E4	11100100	▗ (lower right)	GRPH $
229	E5	11100101	▚	GRPH %
230	E6	11100110	▞	GRPH '
231	E7	11100111	▔ (upper)	GRPH Q
232	E8	11101000	▁ (lower)	GRPH W
233	E9	11101001	▏ (left)	GRPH E
234	EA	11101010	▕ (right)	GRPH R
235	EB	11101011	▛	GRPH A
236	EC	11101100	▜	GRPH S
237	ED	11101101	▙	GRPH D
238	EE	11101110	▟	GRPH F
239	EF	11101111	█	GRPH X
240	F0	11110000	┌	GRPH U
241	F1	11110001	─	GRPH P
242	F2	11110010	┐	GRPH O
243	F3	11110011	┬	GRPH I
244	F4	11110100	├	GRPH J
245	F5	11110101	│	GRPH :
246	F6	11110110	└	GRPH M
247	F7	11110111	┘	GRPH >
248	F8	11111000	┴	GRPH <
249	F9	11111001	┤	GRPH L
250	FA	11111010	┼	GRPH K
251	FB	11111011	◤	GRPH H
252	FC	11111100	◢	GRPH T
253	FD	11111101	◥	GRPH G
254	FE	11111110	◣	GRPH Y
255	FF	11111111	▒	GRPH C

Section 6. Description of LSIs

This section contains a description of the following LSI ICs:

- **MSM80C85ARS (CPU)**
- **MSM81C55RS (PIO)**
- **IM6402 (UART)**
- **μPD1990AC (TIMER)**
- **MC14412 (MODEM)**

MSM80C85ARS (CPU)

MSM80C85ARS (80C85) is a one-chip, 8-bit parallel central processing unit (CPU). Its instruction set is fully compatible with the 8080A microprocessor.

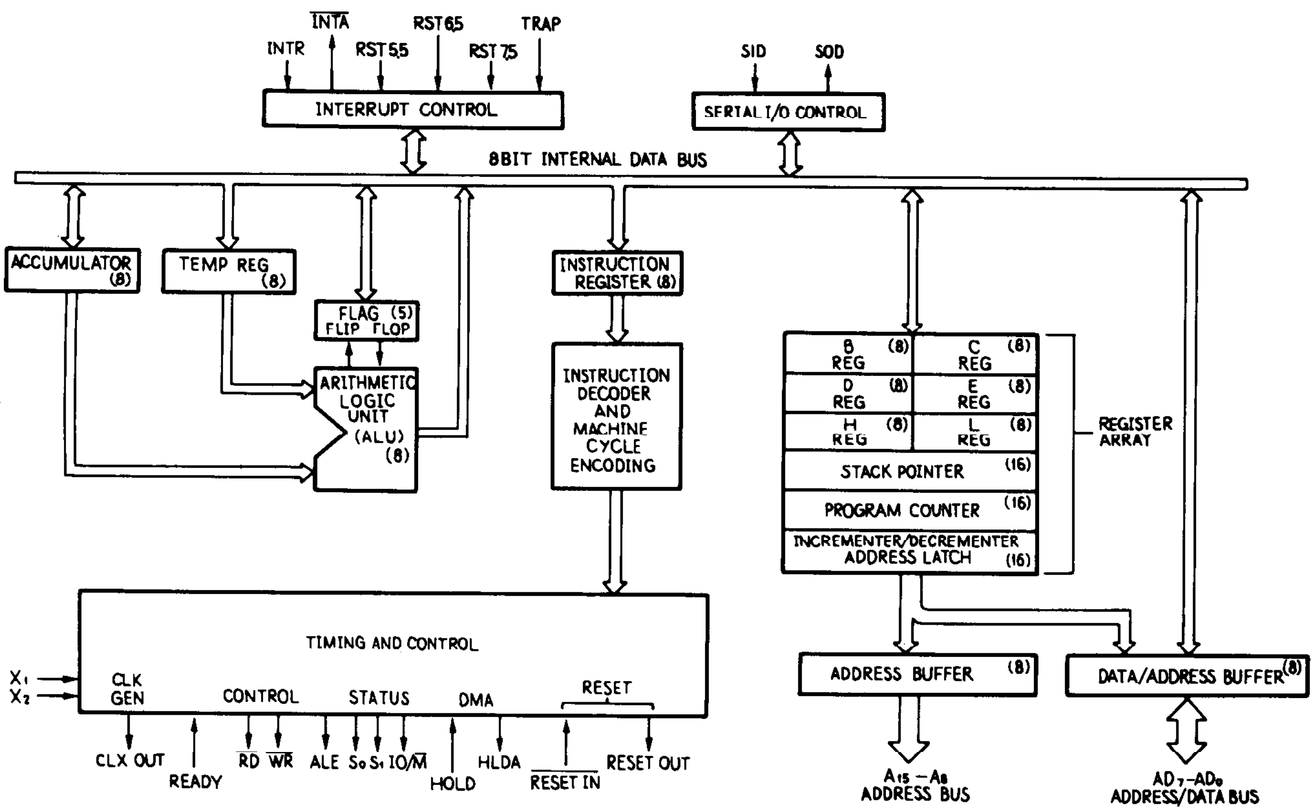


Figure 6-1. 80C85 CPU Functional Block Diagram

Figure 6-2 shows the pin layout of the microprocessor.

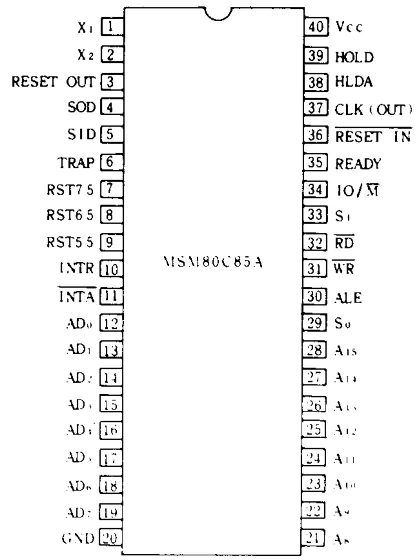


Figure 6-2. 80C85 Pinout Diagram

80C85 Functional Pin Description

Symbol	Function
A_8 - A_{15} (Output, 3-state)	Address Bus: Most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7} (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: Occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and $IO/\overline{M}$ (Output)	Machine cycle status:

$IO/\overline{M}$	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

*** = 3-state (high impedance)**
X = unspecified

Symbol	Function
	S_1 can be used as an advanced $R/\overline{W}$ status. $IO/\overline{M}$, S_0, and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ **(Output, 3-state)**	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ **(Output, 3-state)**	WRITE control: A low level on $\overline{WR}$ indicates data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$, 3-stated during Hold and Halt modes and during RESET.
READY **(Input)**	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.
HOLD **(Input)**	HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer (internal processing can continue). The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and $IO/\overline{M}$ lines are 3-stated.
HLDA **(Output)**	HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and will relinquish the bus in the next clock cycle. HLDA goes low after the HOLD request is removed. The CPU takes the bus one-half clock after HLDA goes low.
INTR **(Input)**	INTERRUPT REQUEST is used as a general purpose interrupt and sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle, a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$ **(Output)**	INTERRUPT ACKNOWLEDGE is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted.
RST 5.5 **RST 6.5** **RST 7.5** **(Inputs)**	RESTART interrupts have same timing as INTR, but cause the automatic insertion of an internal RESTART. The priority of these interrupts, which have a higher priority than INTR, is ordered as shown in Table 6-1. In addition, they may be individually masked out using the SIM instruction.
TRAP **(Input)**	TRAP interrupt is a nonmaskable RESTART interrupt, also recognized as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable and has the highest priority of any interrupt. (See Table 6-1.)

Symbol	Function
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an RC network for power-on RESET delay. The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates the CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line: Data on this line is loaded into accumulator bit 7 when a RIM instruction is executed.
SOD (Output)	Serial output data line: Output SOD is set or reset as specified by the SIM instruction.
Vcc	+5 volt supply.
GND	Ground reference.

Name	Priority	Address Branched to (1) when Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST7.5	2	3CH	Rising edge (latched).
RST6.5	3	34H	High level until sampled.
RST5.5	4	2CH	High level until sampled.
INTR	5	See Note (2)	High level until sampled.

Table 6-1. 80C85 Interrupt Priority, RESTART, ADDRESS, and Sensitivity

Notes:

- The processor pushes the PC on the stack before branching to the indicated address.
- The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

Functional Description

80C85 has twelve addressable 8-bit registers. Four function only as two 16-bit register pairs. Six can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 80C85 register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers: data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

80C85 uses a multiplexed data bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle, the low order address is sent out on the Address/Data Bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle, the data bus is used for memory or I/O data.

80C85 provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD, READY, and all interrupts are synchronized with the processor's internal clock. 80C85 also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, 80C85 has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

80C85 has five interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt, but nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 6-1.)

There are two types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are **high level-sensitive** like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is **rising edge-sensitive**.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then, it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the 80C85. RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

Status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{\text{RESET IN}}$.

Interrupts are arranged in a fixed priority that determines which interrupt is to be recognized (if more than one is pending) as follows: TRAP — highest priority; RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. TRAP input is recognized just as any other interrupt, but has the highest priority. It is not affected by any flag or mask and is both edge and level sensitive. TRAP input must go high and remain high until acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 6-3 illustrates the TRAP interrupt request circuitry within the 80C85. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an E1 instruction is executed.

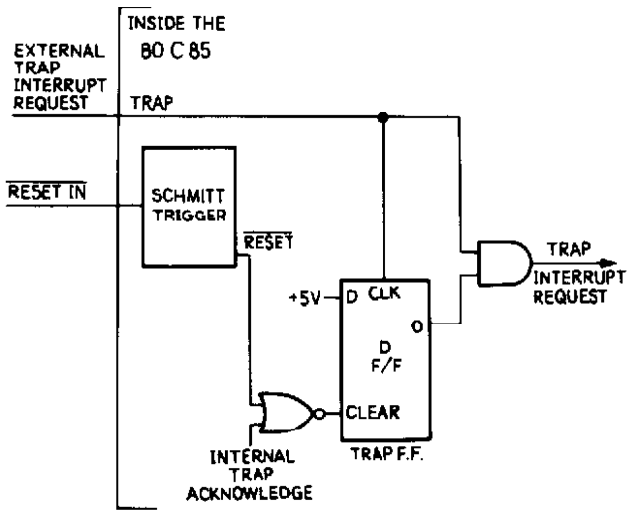


Figure 6-3. 80C85 TRAP and RESET in Circuit

Although TRAP disables interrupts, it preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5-7.5 will provide current Interrupt Enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is ready by RIM, and SIM sets the SOD data.

Basic System Timing

80C85 has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8 bits of address on the Data Bus. Figure 6-4 shows an instruction fetch, memory read, and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O, port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals $\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$. (See Table 6-2.) The status lines can be used as advanced controls (for example, device selection), since they become active at the T_1 state at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time the transfer of data is to take place, and are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the reception of READY or HOLD inputs). Any T state must be one of ten possible states, shown in Table 6-3.

MACHINE CYCLE			STATUS			CONTROL		
			IO/$\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE of INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI):	DAD	0	1	0	1	1	1
		ACK, of RST, TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Table 6-2. 80C85 Machine Cycle Chart

Machine Strate	Status & Buses				Control		
	S_1, S_0	IO/$\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$, $\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"   1 = Logic "1"   TS = High Impedance   X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.

† IO/M = 1 during $T_4 - T_6$ of INA machine cycle.

Table 6-3. 80C85 Machine State Chart

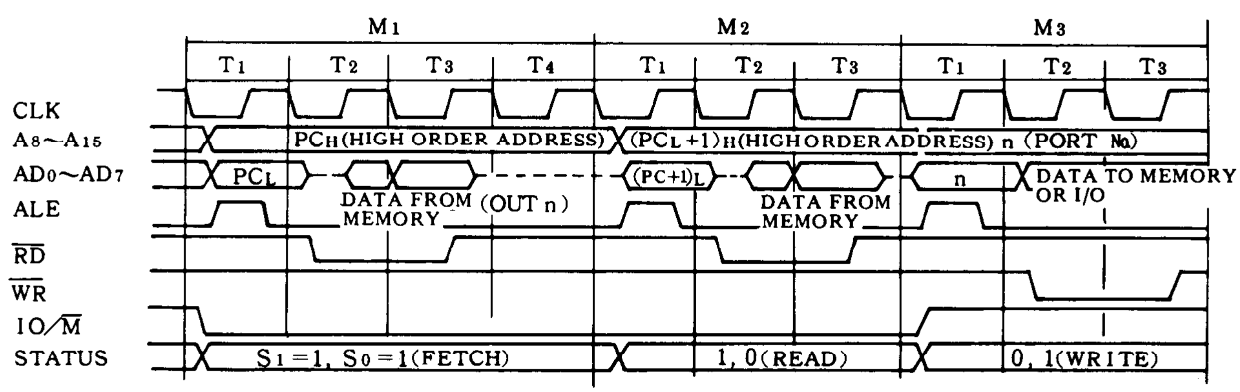


Figure 6-4. 80C85 Basic System Timing

Ambient Temperature Under Bias	−40°C to +85°C
Storage Temperature	−55°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Power Dissipation	1.0 Watt

Table 6-4. 80C85 Absolute Maximum Ratings

80C85 Waveform

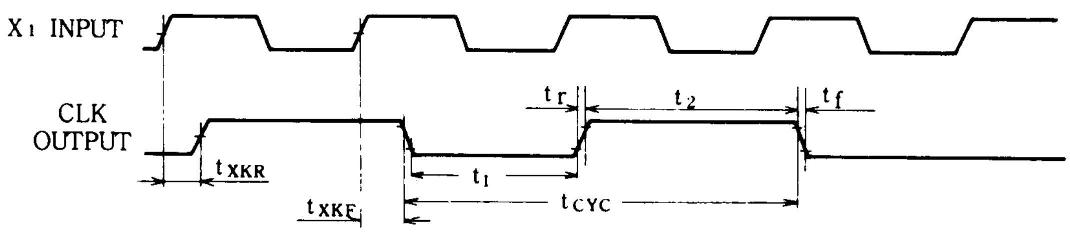
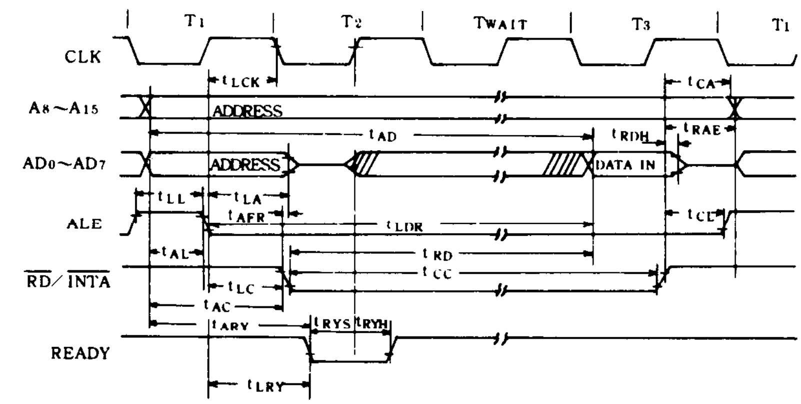
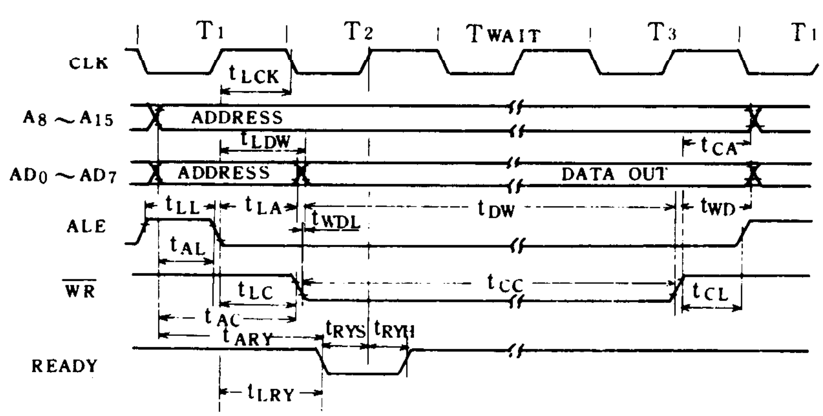


Figure 6-5. 80C85 Clock Timing Waveform

Read Operation



Write Operation



Read Operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation

Figure 6-6. 80C85 Bus Timing

Hold Operation

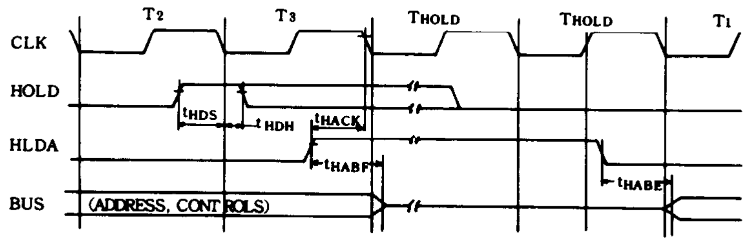
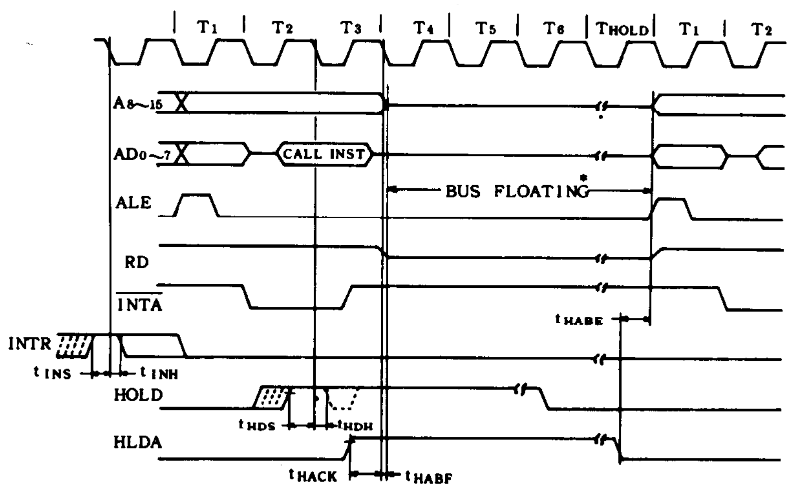


Figure 6-7. 80C85 Hold Timing



* IO/M is also floating during this time.

Figure 6-8. 80C85 Interrupt and Hold Timing

MSM81C55RS (PIO)

C-MOS, 2048-bit STATIC RAM with I/O ports and Timer. The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed as status pins, thus allowing the remaining two ports to operate in the handshake mode.

A 14-bit programmable counter/timer is also included on the chip to provide either a square wave or terminal count pulse for the CPU system, depending on the timer mode.

81C55 RAM is not used in the Tandy 102. A timer/counter is used as the clock generator necessary for communication and to generate the melody.

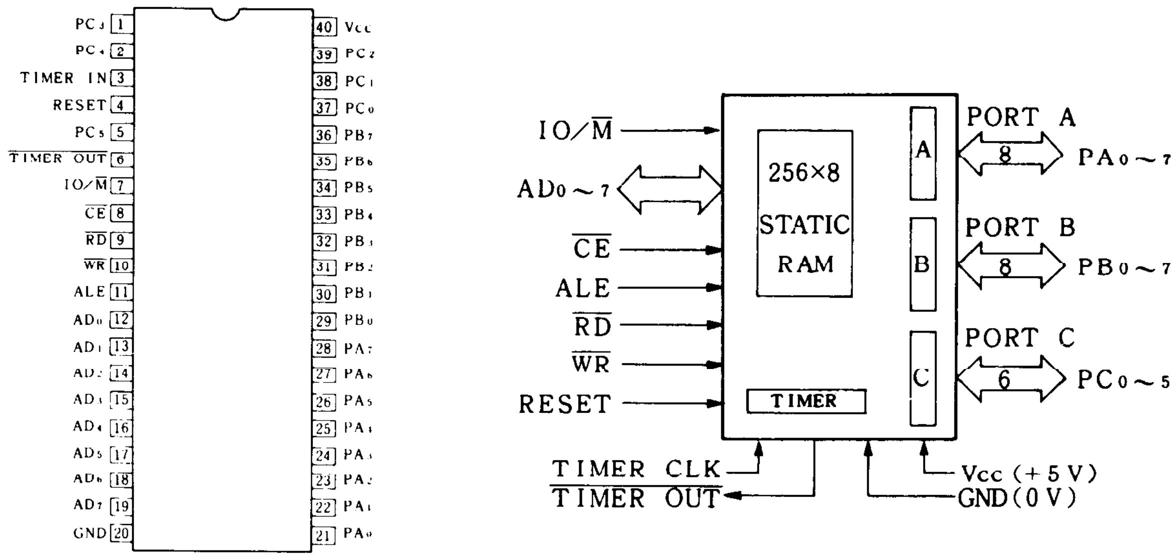


Figure 6-9. 81C55 Pin Configuration and Block Diagram

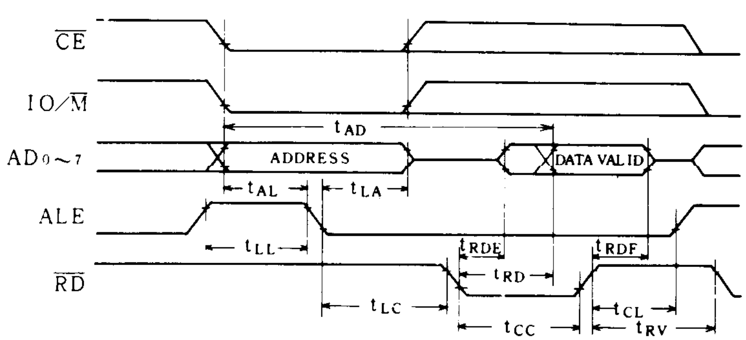
81C55 Pin Functions

Symbol	Function
RESET (Input)	Pulse provided by the 80C85 to initialize the system (connect to 80C85 RESET OUT). A high input on this line resets the chip and initializes the three I/O ports to input mode. Width of the RESET pulse should typically be two 80C85 clock cycle times.
AD_{0-7} (Input)	Three-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside 81C55 on the falling edge of ALE. The address can be either for the memory section or the I/O section, depending on the IO/$\overline{M}$ input. 8-bit data is either written into the chip or read from the chip, depending on $\overline{WR}$ or $\overline{RD}$ input signal.
CE (Input)	Chip Enable: $\overline{CE}$ is ACTIVE LOW.
$\overline{RD}$ (Input)	Read control: Input low on this line with the Chip Enable active enables AD_{0-7} buffers. If the IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (Input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data Bus to be written to the RAM or I/O ports and command/status register depending on the IO/$\overline{M}$.
ALE	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (Input)	Selects the memory if low, and the command/status registers if high.

Symbol	Function
PA$_{0-7}$ (8) (Input/Output)	These eight pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB$_{0-7}$ (8) (Input/Output)	These eight pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC$_{0-5}$ (6) (Input/Output)	These six pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When used as control signals, PC$_{0-5}$ provide the following: PC$_0$ — A INTR (Port A Interrupt) PC$_1$ — ABF (Port A Buffer Full) PC$_2$ $\overline{\text{A STB}}$ (Port A Strobe) PC$_3$ — B INTR (Port B Interrupt) PC$_4$ — $\overline{\text{B BF}}$ (Port B Buffer Full) PC$_5$ — B STB (Port B Strobe)
TIMER IN (Input)	Input to the counter-timer.
$\overline{\text{TIMER OUT}}$ (Output)	Timer output. This output can be either a square wave or a pulse, depending on the timer mode.
Vcc	+5 volt supply.
GND	Ground reference.

81C55 Waveform

Read Cycle



Write Cycle

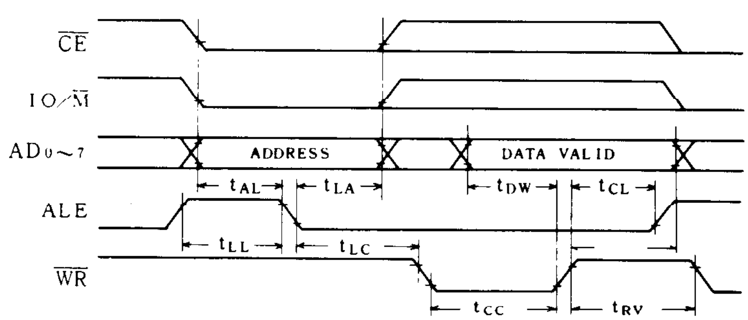
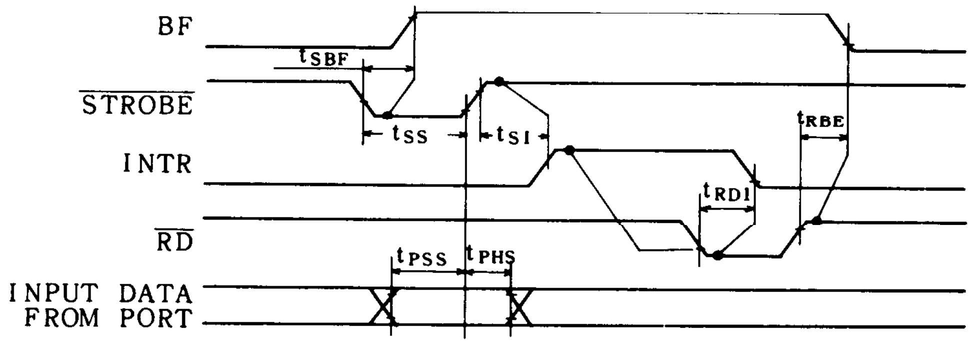


Figure 6-10. 81C55 Read/Write Timing Diagram

81C55 Strobed I/O Timing

Strobed Input Mode



Strobed Output Mode

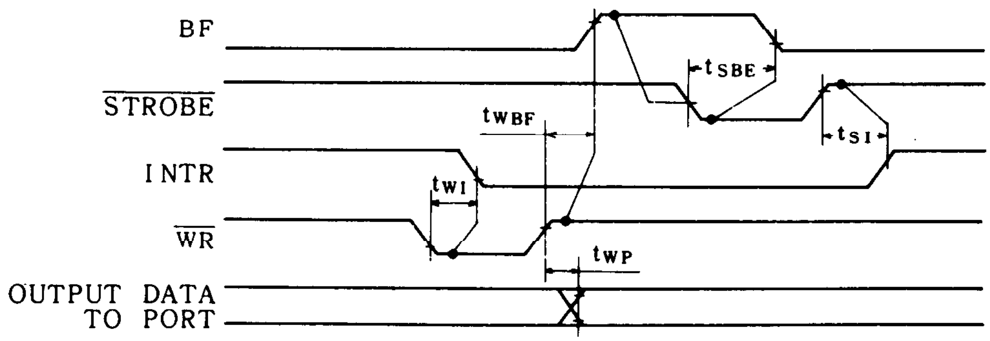
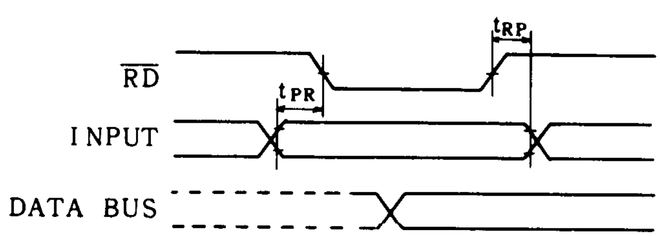


Figure 6-11. 81C55 Strobed I/O Timing

81C55 Basic I/O Timing

Basic Input Mode



Basic Output Mode

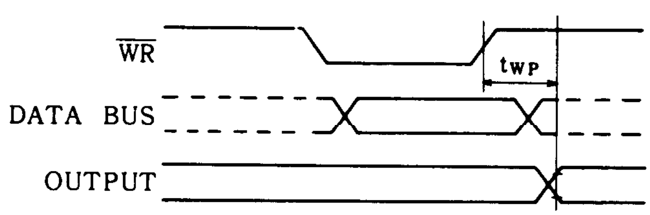
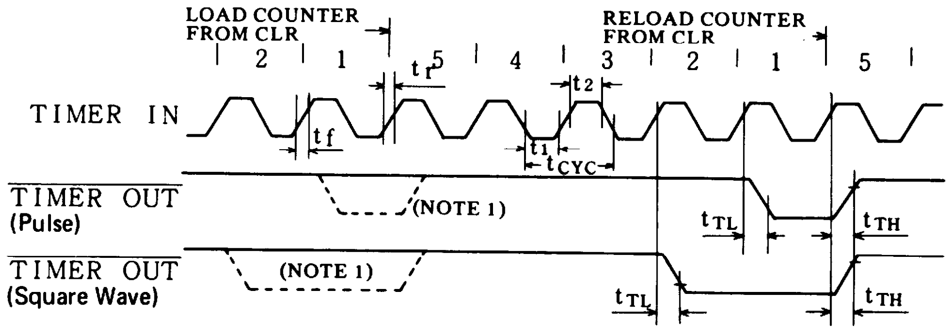


Figure 6-12. Basic I/O Timing



NOTE: The timer output is periodic if in an automatic reload mode (M1 MODE BIT = 1)

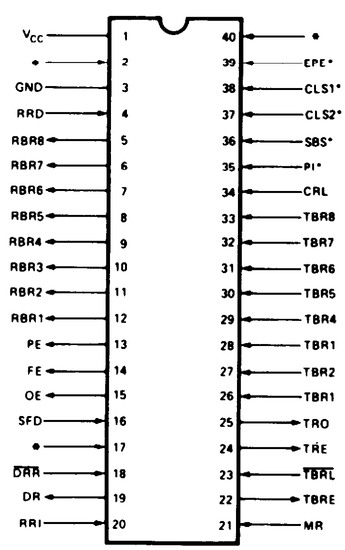
Figure 6-13. 81C55 Timer Output Waveform (Countdown from 5 to 1)

IM6402 (UART)

IM6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity, and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

Data word length can be 5, 6, 7, or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. Stop bits may be one or two, or one and one-half when transmitting a 5-bit code.

IM6402 can be used in a wide range of applications, including modems, printers, peripherals, and remote data acquisition systems. CMOS/LSI technology permits operation clock frequencies up to 2.0 MHz (125K baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300 mW to 10 mW. Status logic increases flexibility and simplifies the user interface.



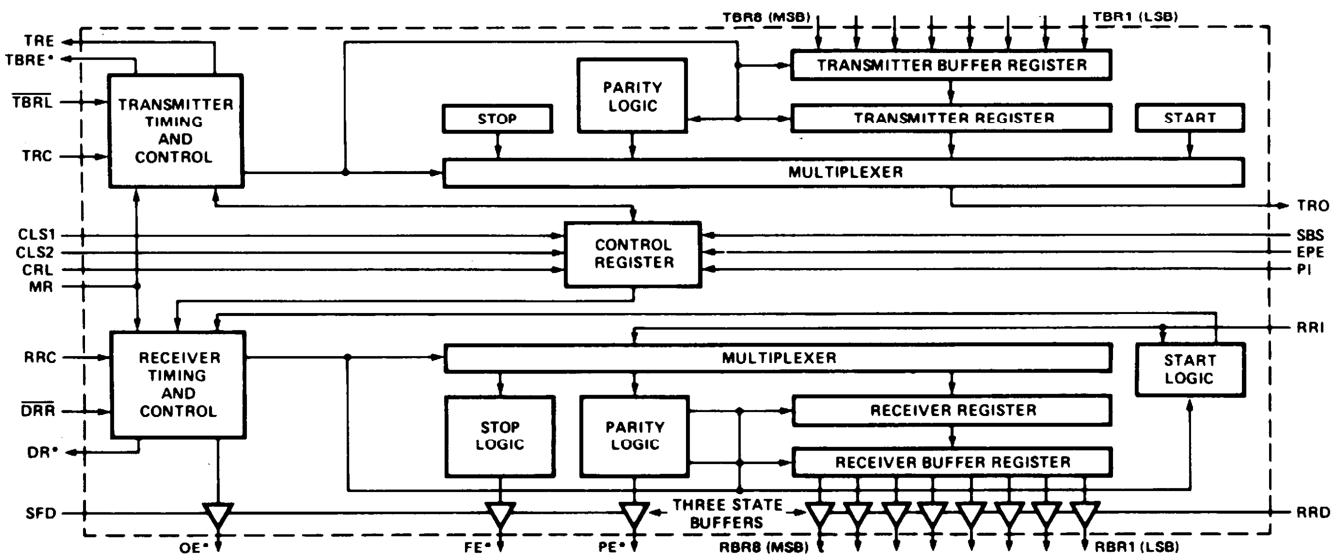
* Shown in Table 6-5

Figure 6-14. IM6402 Pin Layout

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

Table 6-5. IM6402 Control Word Format



*These outputs are three state (IM6402) or always active (IM6403)

Figure 6-15. IM6402 Functional Block Diagram

IM6402 Pin Functions

Symbol	Description
Vcc	Positive voltage supply
NC	No connection
GND	Ground
RRD	High level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1-RBR8 to a high impedance state.

Symbol	Description
RBR8	Contents of the RECEIVER BUFFER REGISTER appear on these 3-state outputs. Word formats of less than eight characters are justified to RBR1.
RBR7	See Pin 5 - RBR8
RBR6	See Pin 5 - RBR8
RBR5	See Pin 5 - RBR8
RBR4	See Pin 5 - RBR8
RBR3	See Pin 5 - RBR8
RBR2	See Pin 5 - RBR8
RBR1	See Pin 5 - RBR8
PE	High level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited, this output is low.
FE	High level on FRAMING ERROR indicates the first stop bit was invalid.
OE	High level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the received buffer register.
SFD	High level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
RRC	RECEIVER REGISTER CLOCK is 16X the receiver data rate.
DRR	Low level on DATA RECEIVED RESET clears the data received output DR to a low level.
DR	High level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
MR	High level on MASTER RESET clears PE, FE, GE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the receiver buffer register. This input must be pulsed at least once after power-up.
TBRE	High level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
TBRL	Low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register is busy. Transfer is automatically delayed so that the two characters are transmitted end to end.

Symbol	Description
TRE	High level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character, including stop bits.
TRO	Character data, start data, and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
TBR2	See Pin 26 - TBR1
TBR3	See Pin 26 - TBR1
TBR4	See Pin 26 - TBR1
TBR5	See Pin 26 - TBR1
TBR6	See Pin 26 - TBR1
TBR7	See Pin 26 - TBR1
TBR8	See Pin 26 - TBR1
CRL	High level on CONTROL REGISTER LOAD loads the control register.
PI	High level on PARITY INHIBIT inhibits parity generation. Parity checking forces PE output low.
SBS	High level on STOP BIT SELECT selects 1.5 stop bits for 5-character format and 2 stop bits for other lengths.
CLS2	These inputs program the CHARACTER LENGTH SELECTED — CLS1 low CLS2 low, 5 bits; CLS1 high CLS2 low, 6 bits; CLS1 low CLS2 high, 7 bits; CLS1 high CLS2 high, 8 bits.
CLS1	See Pin 37 - CLS2.
EPE	When P1 is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
TRC	TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

µPD1990AC (TIMER)

µPD1990AC is a CMOS integrated circuit with a clock function designed for connection to a microcomputer.

This IC independently measures the month, date, day of the week, hour, minute, and second, and inputs and outputs time data freely upon command from the microprocessor. By employing this IC, the microprocessor is freed from performing clock functions and can be devoted exclusively to other complex operations.

µPD1990C employs the oscillation of a 32.768 kHz crystal as a reference. All functions are enclosed in a 14-pin dual in-line package.

Features

- Measures time (hours, minutes, and seconds) and calendar (months, dates, and days of the week).
- Inputs and outputs serial data. (Input and output code: all digits are binary coded decimals, except the month, which is a hexadecimal code.)
- Generates reference frequency of 32.768 kHz through the crystal oscillator circuit.
- Provides timing pulse outputs. (Selection of 64 Hz, 256 Hz, or 2048 Hz is possible.)
- Makes multi-chip applications possible by using the CS (chip selection) terminal.

Specifications

Reference frequency (XTAL osc.)	32.768 kHz
Date	Hours, minutes, seconds, months, dates, and days of the week ("hours" by 24-hour system) with automatic adjustment of long and short months.
Data (serial input/output and clock)	Data input and output in synchronization with the clock input from CLK.
Time pulse output	Either 64, 256, or 2048 Hz can be selected by command.
Mode selection	Selected according to input C_0-C_2. C_2 = 0 Register control (control of data input/output). C_2 = 1 TP control (control of time pulses) and test control (control of test mode). Commands are latched by the STB (strobe) input.
Chip select	CLK and STB inputs are prohibited by CS input.
Prohibition of data output	DATA OUT terminal will become high impedance when the OUT ENABL is input. Has no relation with other actions.

Terminals

Input terminals

DATA IN	Data input of 40-bit shift register
CLK	Shift clock input of 40-bit shift register
C_0-C_2	Command input (3-bit)
STB	Strobe input
CS	Chip select input (prohibits CLS and STB)
OUT ENBL	Output control input (makes the DATA OUT high impedance by inputting low level).

Output terminals

DATA OUT	Data output of 40-bit shift register.
TP	Time pulse output.

Oscillation terminals

XTAL 1	Oscillation inverter input (OSC IN).
XTAL 2	Oscillation inverter output (OSC OUT).

Power supply terminals

VDD	Plus power supply
GND (Vss)	Common line

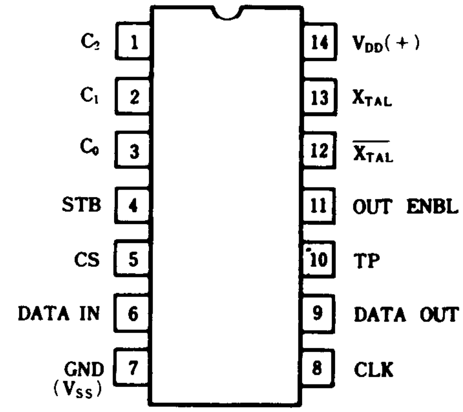


Figure 6-16. µPD1990AC Pin Layout

Block Diagram

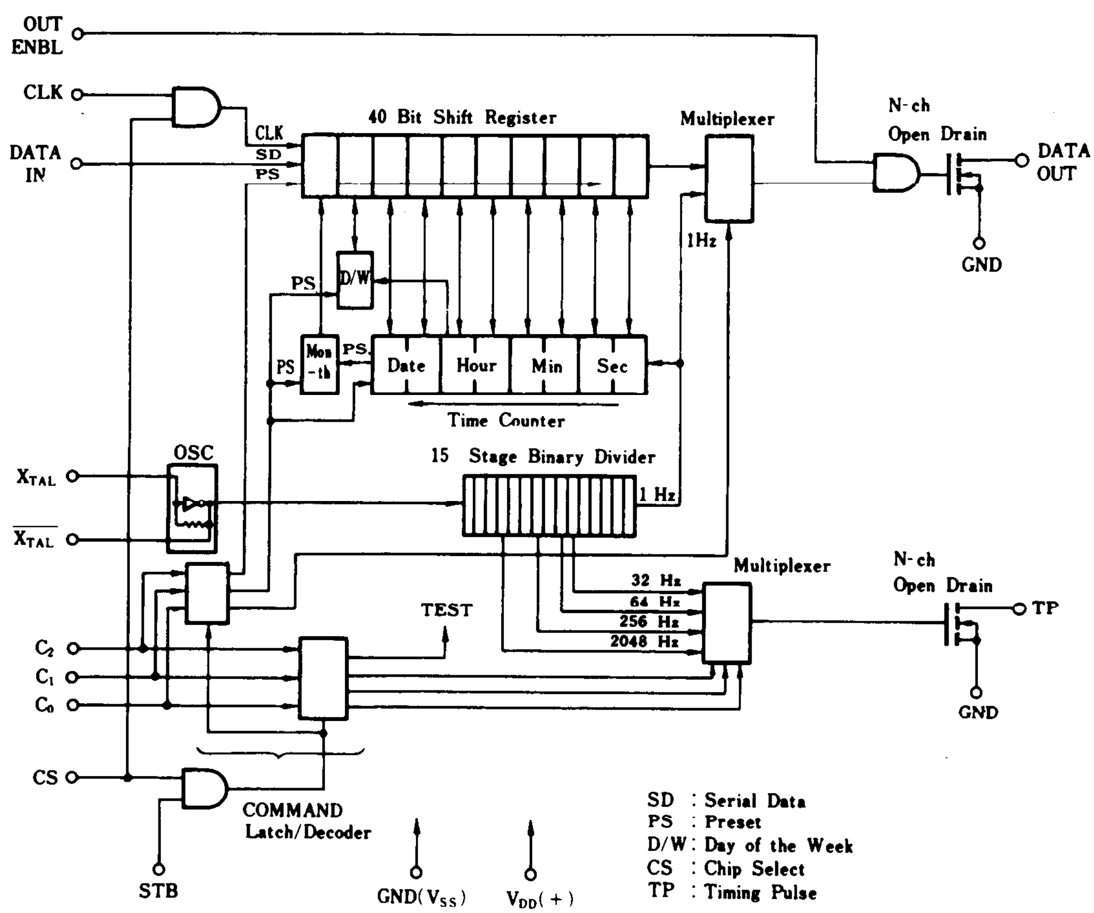


Figure 6-17. µPD1990AC Block Diagram

Command Input Timing Diagram

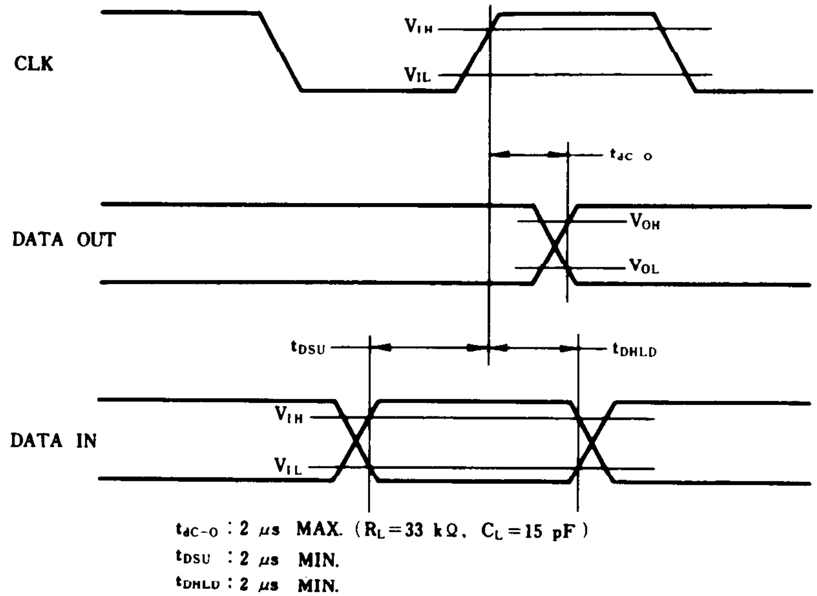


Figure 6-18. μPD1990AC Command Input Timing Diagram

Commands designated by C_0, C_1, and C_2 will be written into the latch when the STB terminal becomes high level, and will be held until a different command of the same group is written in.

Data Input/Output Timing Diagram

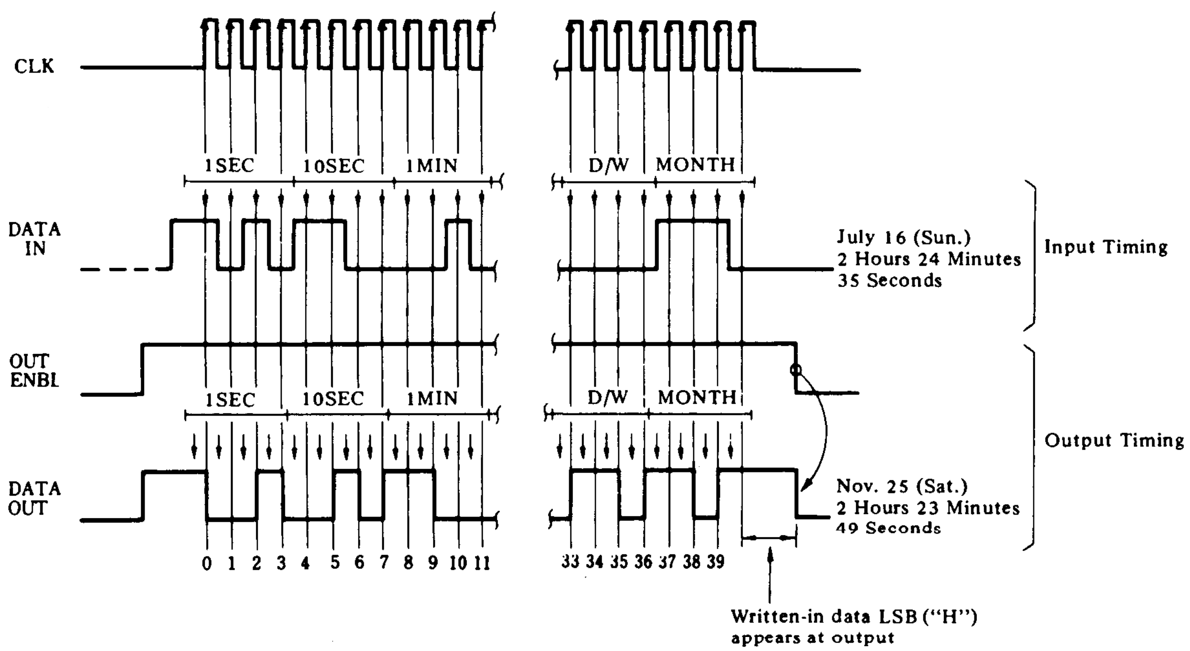


Figure 6-19. μPD1990AC Data Input/Output Timing Diagram

MC14412 (MODEM)

Figure 6-22 shows the MODEM in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before dividing the 600 ohm telephone line.

The FSK signal from the remote MODEM is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal.

The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

Pin Functions

Symbol	Function
TYPE	TYPE input selects either the U.S. or C.I.T.T. operational frequencies for both transmitting and receiving data. When TYPE input = "1", the U.S. standard is selected and when the TYPE input = "0", the C.I.T.T. standard is selected.
Tx Data	Transmission Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating the U.S. standard (TYPE = 1), a logic 1 input level represents a Mark or when operating in the C.I.T.T. standard (TYPE = 0), a logic 1 input level represents a Mark.
Tx Car	Transmit Carrier is a digitally-synthesized sine wave derived from a 1.0 MHz oscillator reference. Frequency characteristics are:

United States Standard Transmit Frequency — **TYPE = 1, ECHO = 0**

Mode	Tx Data	Tx Car
Originate 1	Mark 1	1270 Hz
Originate 1	Space 0	1070 Hz
Answer 0	Mark 1	2225 Hz
Answer 0	Space 0	2025 Hz

C.C.I.T.T. Standard Transmit Frequency — **TYPE = 0, ECHO = 0**

Channel 1	Mark 1	980 Hz
No. 1 1	Space 0	1180 Hz
Channel 0	Mark 1	1650 Hz
No. 2 0	Space 0	1850 Hz

Echo Suppressor Disable Tone — **TYPE = 0, ECHO = 1**

Chan. No. 2 0	1	2100 Hz

Symbol	Function
Tx Enable	Transmit carrier output is enabled when the Tx Enable input = 1. No output tone can be transmitted when Tx Enable = 0.
MODE	Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When Mode = 1, the U.S. originate mode is selected (Type input = 1) or the C.C.I.T.T. channel No. 1 (Type = 0). When Mode = 0, the U.S. answer mode is selected (Type = 1) or the C.C.I.T.T. channel No. 2 (Type input = 0).
ECHO	When Echo input = 1 (Type = 0, Mode = 0, Tx Data = 1) the demodulator will transmit a 2100 Hz tone for the disabling line echo suppressors. During normal data transmission, this input should be low = 0.
Rx Data	Receive Data output is the digital data resulting from demodulating the Receive Carrier.
Rx Car	Receive Carrier is the FSK input to the demodulation. This input must have either CMOS or TTL compatible logic level input (see TTL pull up disable) at a duty cycle of 50% + −4%, that is a square wave resulting from a signal limiter.
Rx Rate	The demodulator has been optimized for signal to nose performance at 200, 300, and 600 bps. The Receive Carrier must change frequency for more than half of the selected data rate period before the Receive Data output will change.

Data Rate	Rx Rate	Type
0-200 bps	1	0
0-300 bps	1	1
0-600 bps	0	1

SELF TEST	When a high level (ST = 1) is placed on this input, the demodulator is switched to the modulator frequency.
Reset	This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = 1) — otherwise, it should be tied low (0).
Osc in, Osc out	A 1.0 MHz crystal is required to utilize the on-chip oscillator. A 1.0 MHz square wave clock can also be aplied to the Osc in input to satisfy the clock requirement. When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be < 9 PF at the crystal input.
TTLD	To improve TTL interface compatibility, all inputs to the MODEM have controllable P-channel devices which act as pull-up registers when TTLD input is low (0). When the input is taken high (1), the pull up is disabled, thus reducing power dissipation when interfacing with CMOS.

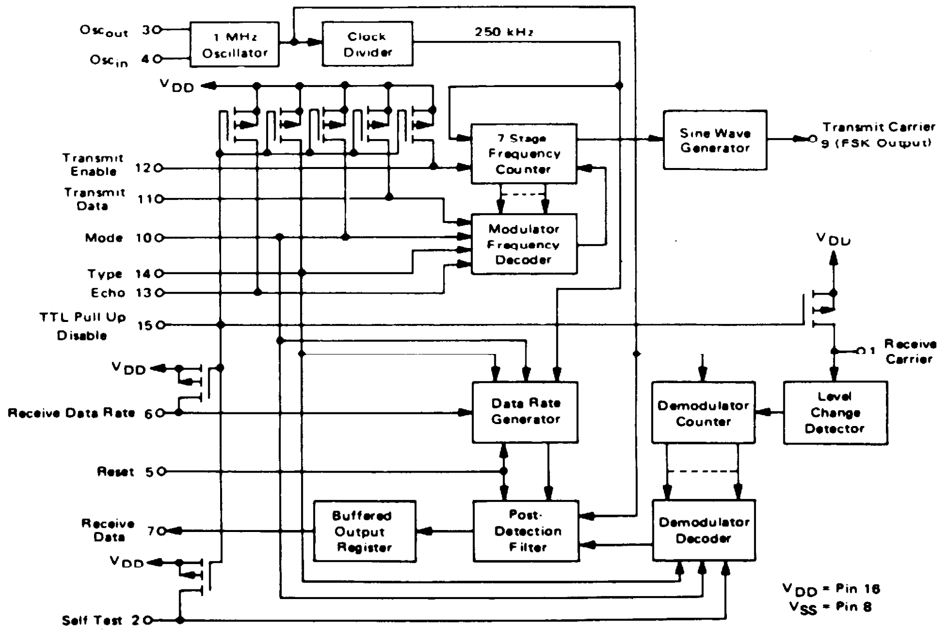


Figure 6-20. MC14412 System Block Diagram

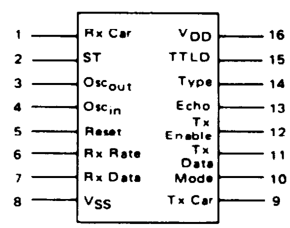


Figure 6-21. MC14412 Pin Layout

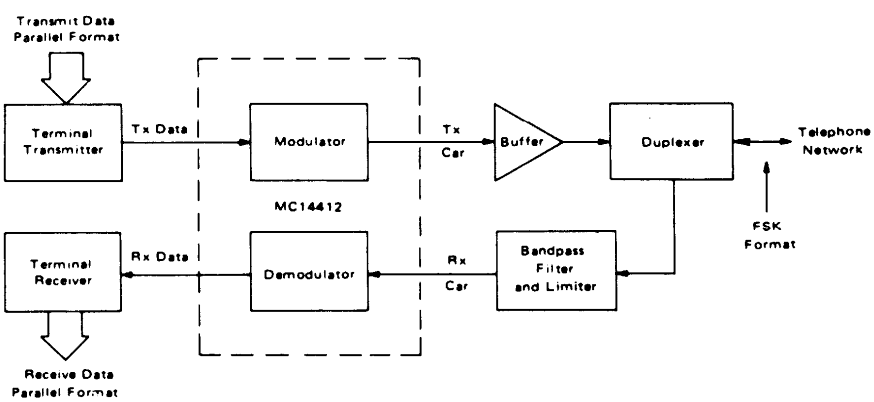


Figure 6-22. MC14412 Application Diagram

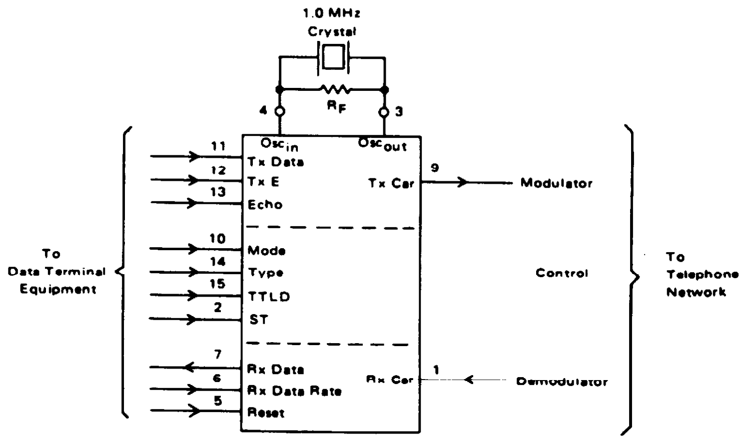


Figure 6-23. MC14412 Input/Output Signals

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